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GAO BTX (Version: A00)

CPU: Intel Conroe, Wolfdale processors in LGA775 Package.

Notice that Apart from PRD Requirement CPU will support Yorkfield as well.

System Chipset:

North Bridge ... Eaglelake-Q43-A3
South Bridge ... ICH10D-B0

Main Memory:

Dual Channel / DDR-II * 4 (Maximum to 8GB)

On Board Device:

Clock Generator ... IDTCV184-2BPAG
Super I/O ... SMSC5524/5514E
LAN ... Boazman 82567-B0
HDA Codec ... AD1984A-04
BIOS ... SPI Flash ROM-32M

Expansion Slots:

PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT * 1
PCI SLOT * 2

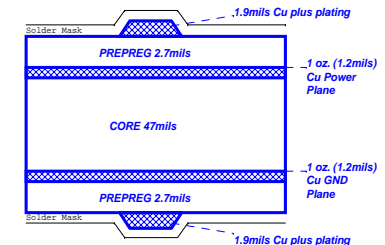
PWM Controller:

Controller ... ADP3293 (3Phase)
Driver ... ADP3120AJRZ

POP1	Proto Build	XDP, LPC HDR, SPI Debug
POP3	SIO SMSC 5524C	
POP4	SIO SMSC 5514E	
POP5	TPM STMicro(4.4mm)	
POP6	TPM Z(6.1mm)	
POP7	TPM J(6.1mm)	
POP8	TPM Winbond(4.4mm)	
POP9	QFN	

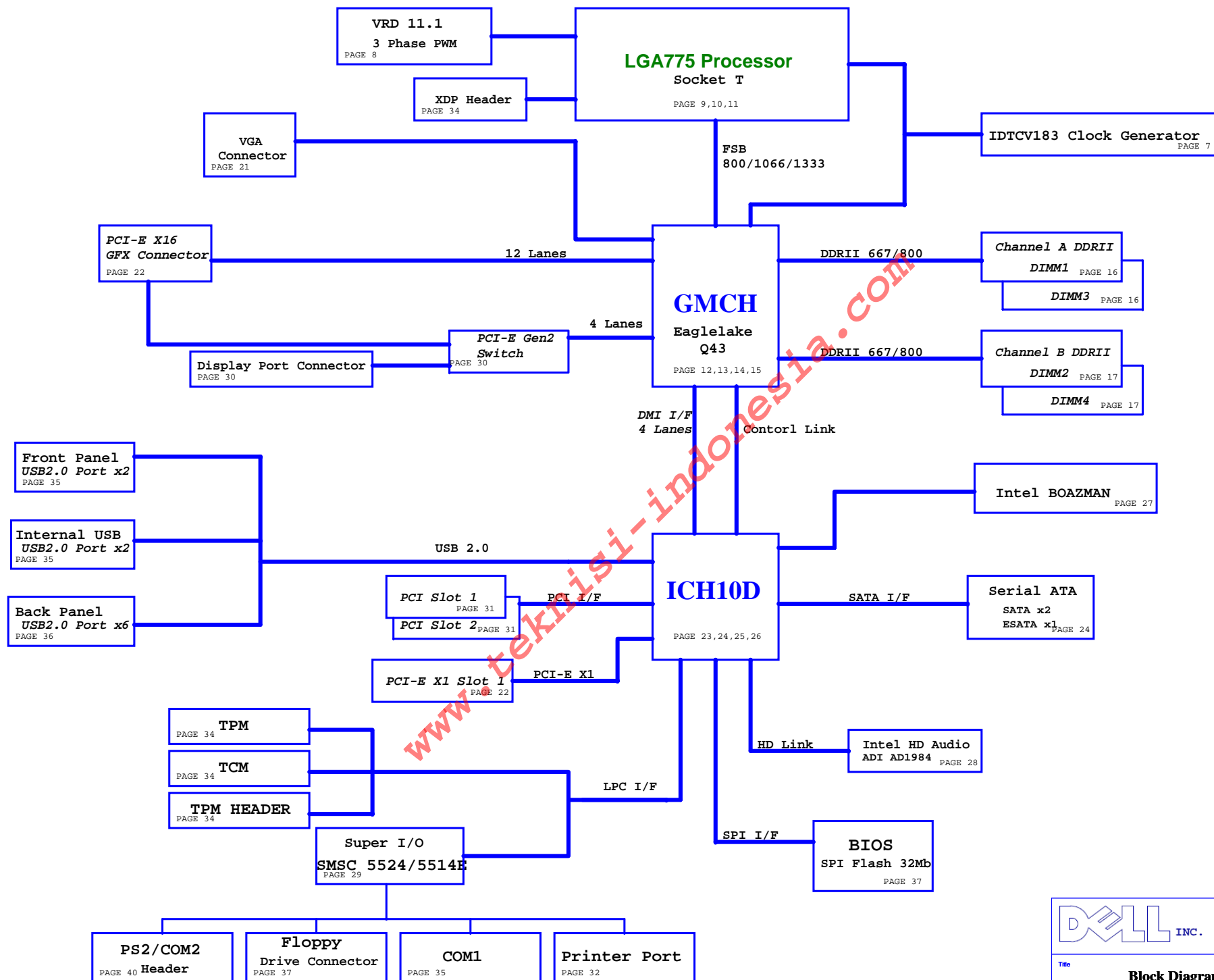
Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
PCIE - 85ohm : 15/4/8/4/15
DMI - 95ohm : 15/4/8/4/15
LAN - 95ohm : 15/4/8/4/15

DELL INC.	
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14.318MHz

CPU

CPU 200/266/333 MHz Diff Pair

MCH 200/266/333 MHz Diff Pair

PCI Express 100 MHz Diff Pair

PCI Express x16 Gfx

DOT 96 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

USB/SIO 48 MHz

ICH 33 MHz

REF 14 MHz

CK PCI STOP

CK CPU STOP

PCI 33 MHz

PCI Slot 1

PCI 33 MHz

PCI Slot 2

TPM 33 MHz

TPM 1.2

Boazman LAN

SIO 33 MHz

SATA 100 MHz Diff Pair

PCI Express 100 Mhz Diff Pair

PCI Express 100 Mhz Diff Pair

GMCH
Eaglelake

DDRII 4 Slots 12 Diff CLKs

Channel A DDRII DDRII 667/800

DIMM1

DIMM2

Channel B DDRII DDRII 667/800

DIMM3

DIMM4

ICH10


Azalia Bit Clock

32.768KHz

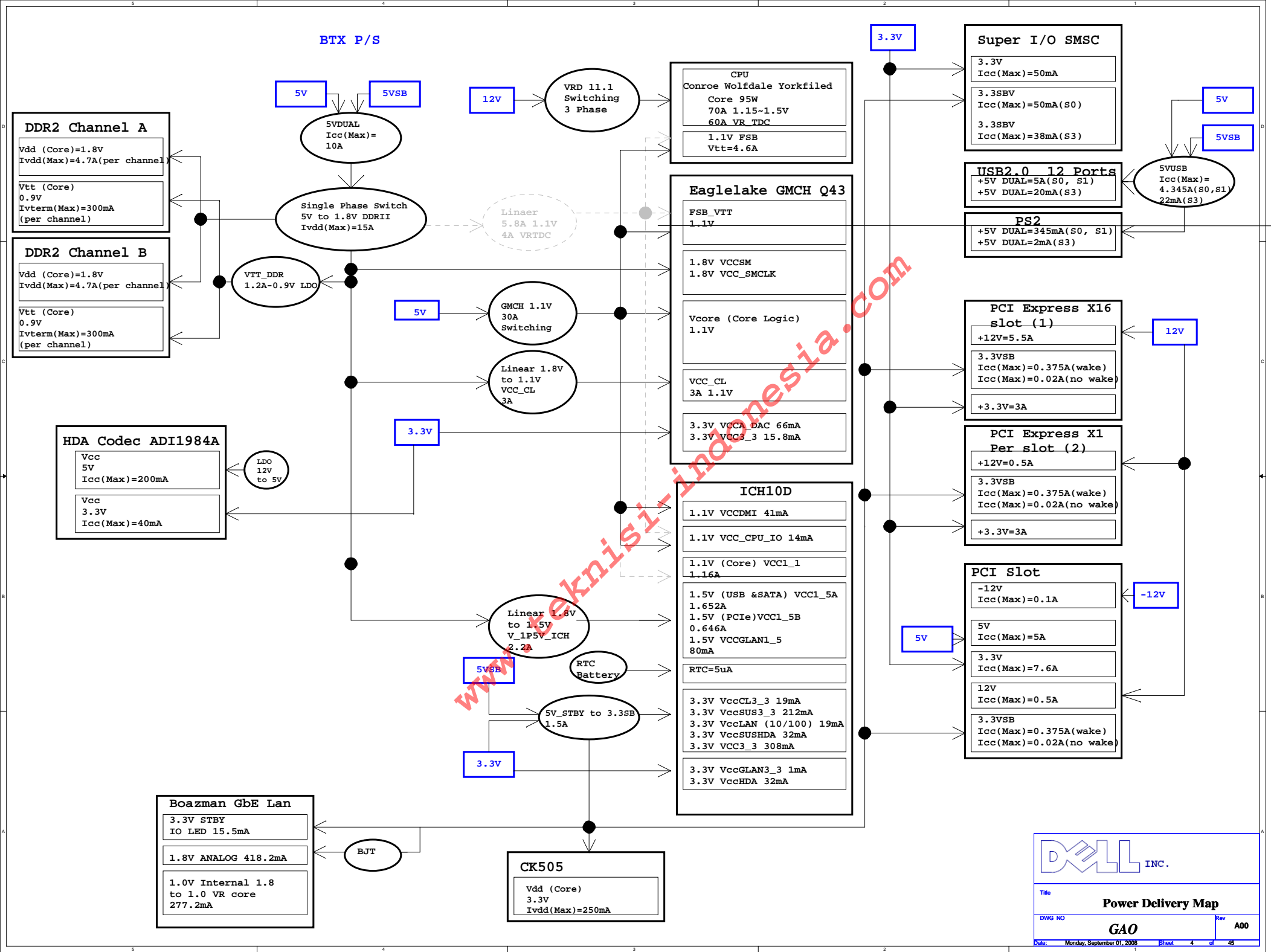
Super I/O

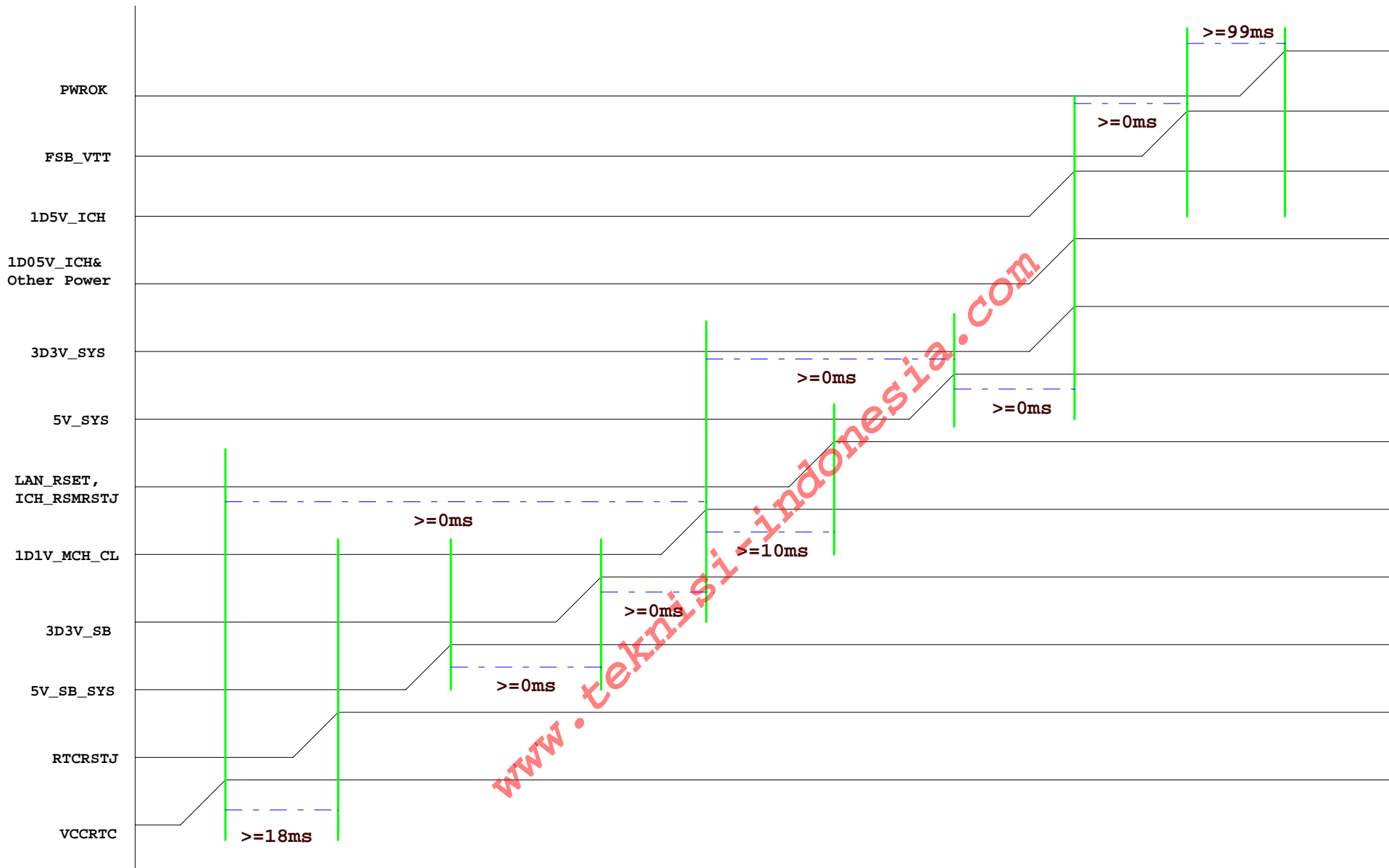
HD Audio

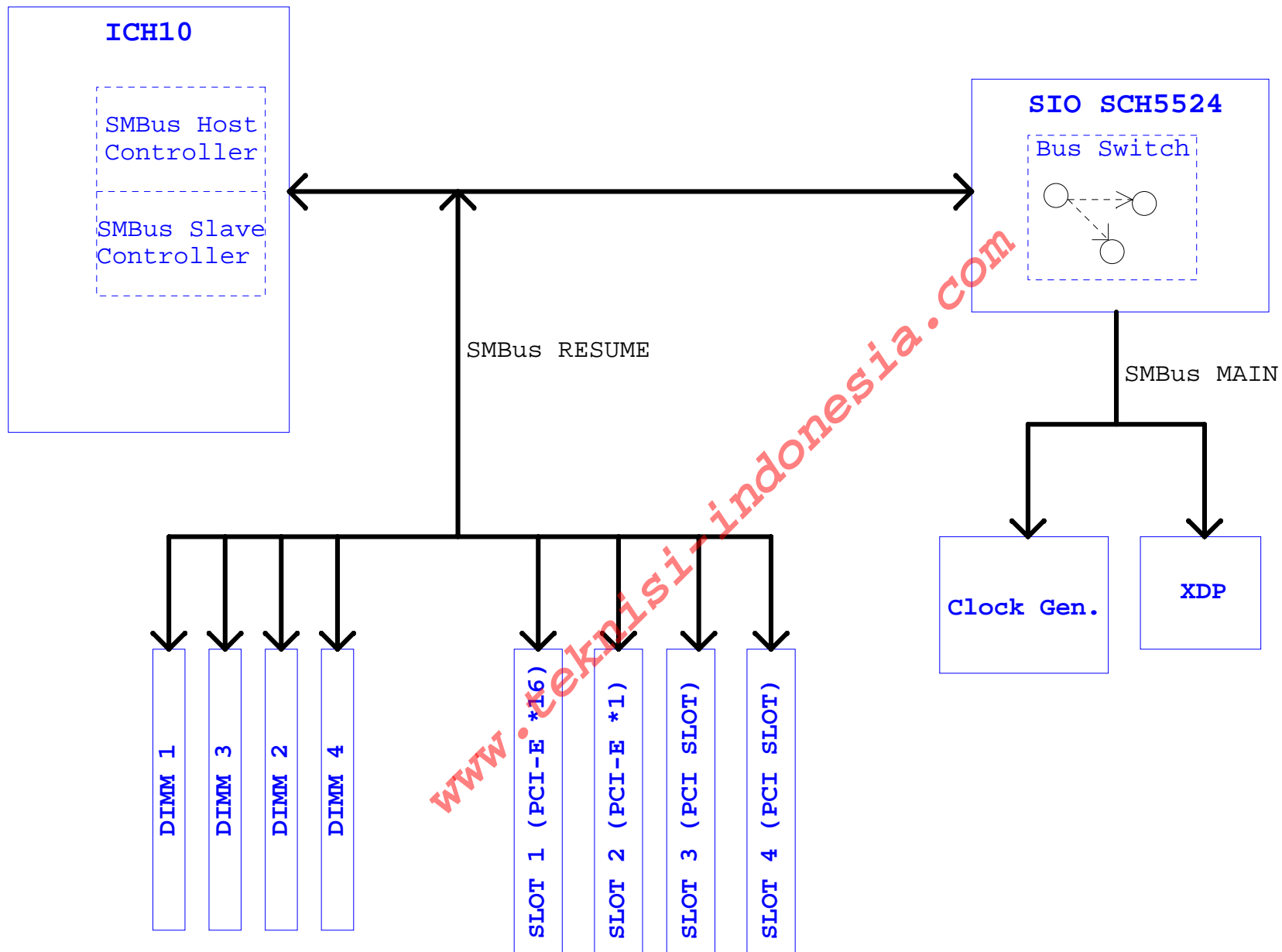
IDT CV184 ClockGen

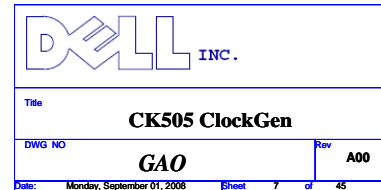
 INC.	
Title	
Clock Distribution	
DWG NO	Rev
GAO	A00
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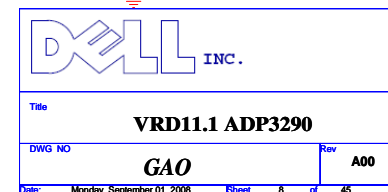
BTX P/S

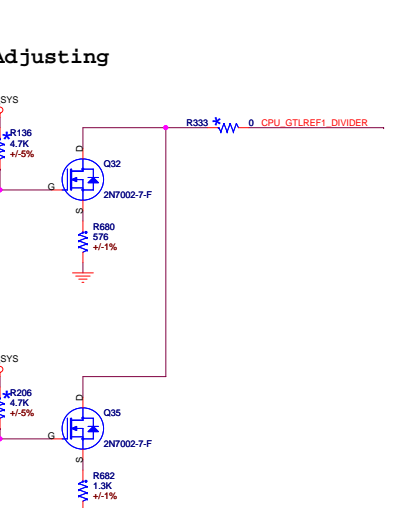
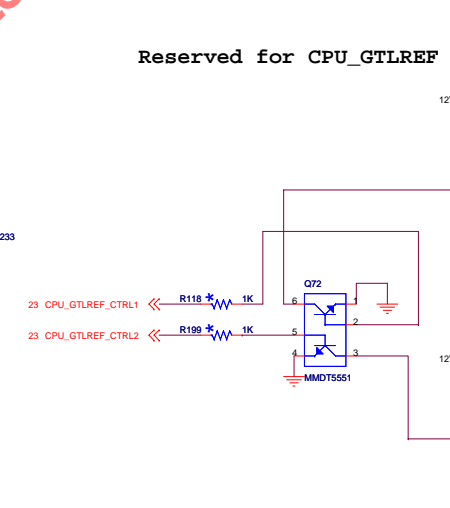
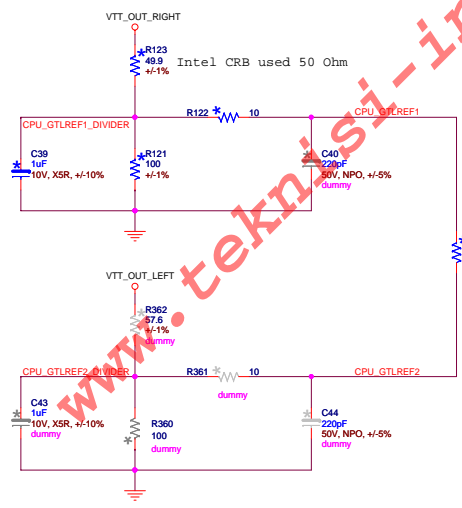
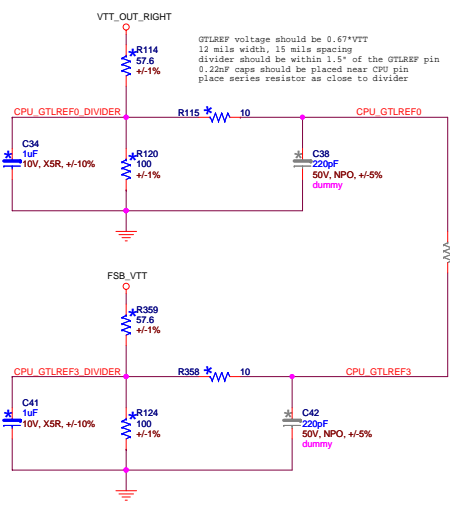
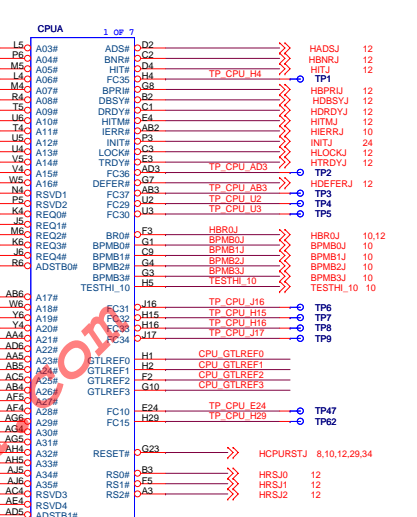
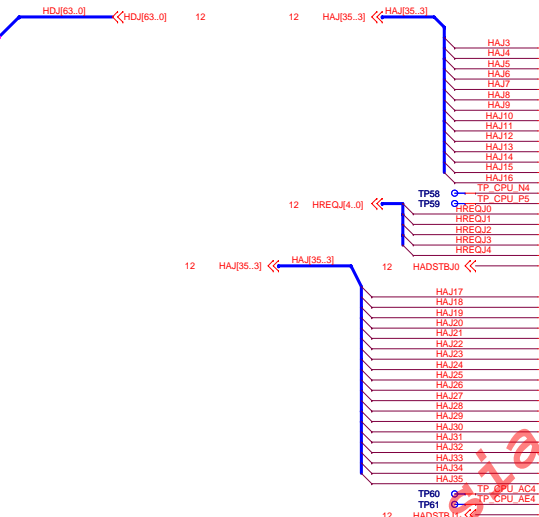
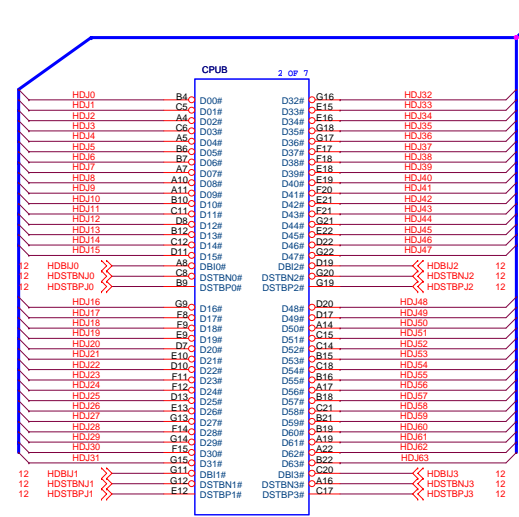












CPU_GTLREF_CTRL1 GP60	CPU_GTLREF_CTRL2 GP18 / 20	GTLREF
0	0	0.615 x Vtt
0	1	0.63 x Vtt
1	0	0.65 x Vtt
1	1	0.67 x Vtt

Default Value

INC.

Title

LGA775 -1

DWG NO

GAO

Rev

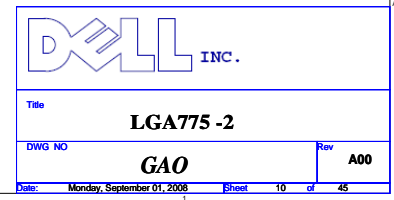
A00

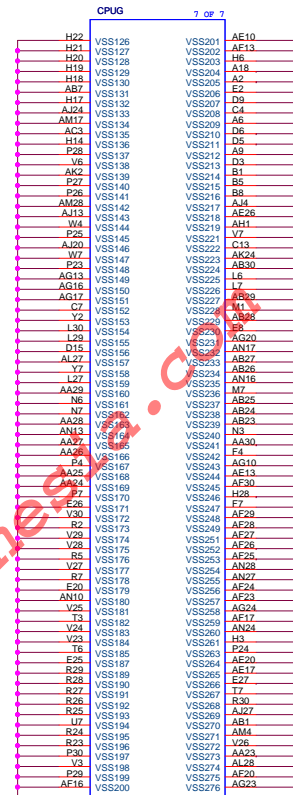
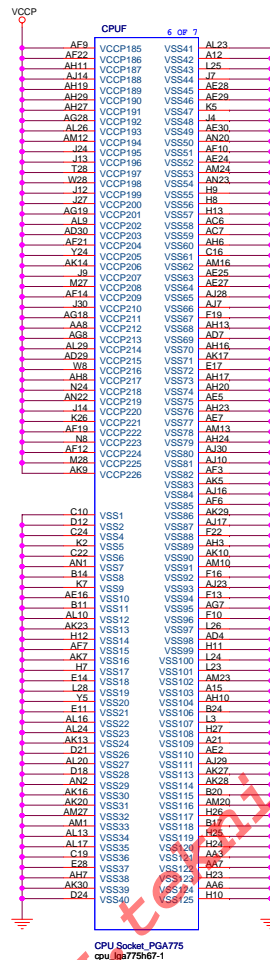
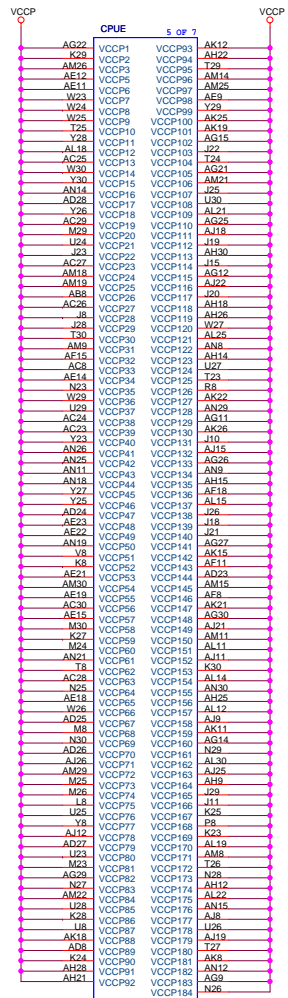
Date

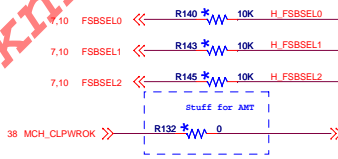
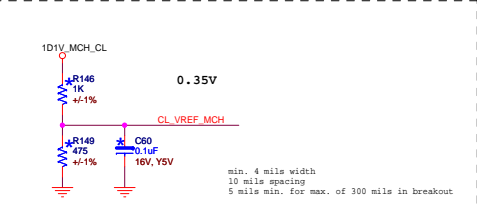
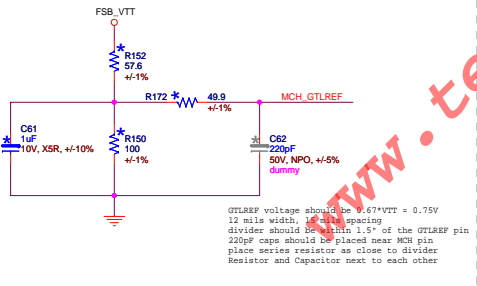
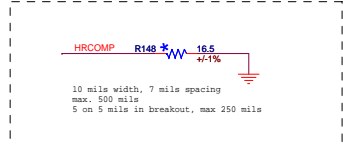
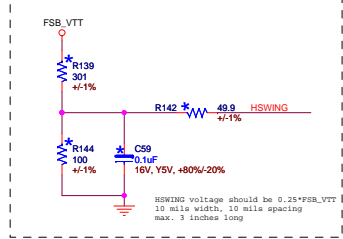
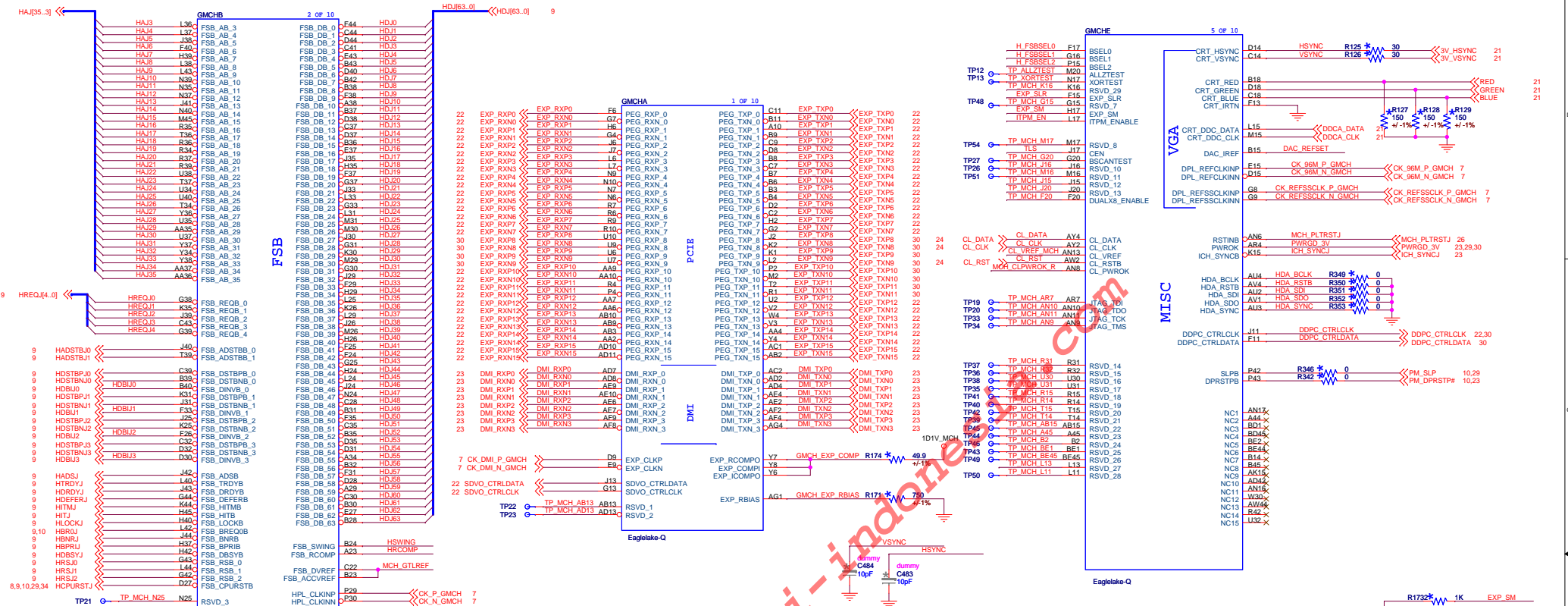
Monday, September 01, 2008

Sheet

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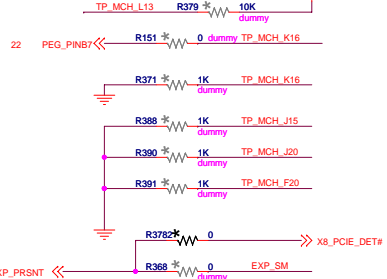
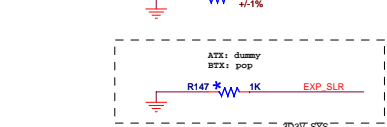






R370 unstuff for enable TLS,
R370 stuff for disable TLS

R545 stuff for enable iTPM,
R545 unstuff for disable iTPM

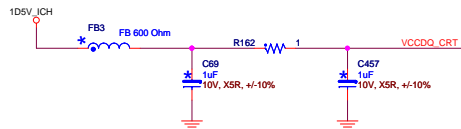


INC.

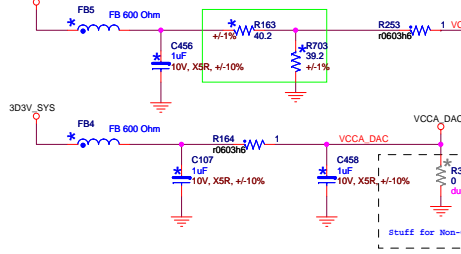
Eaglelake -GMCH -1

DWG NO Rev **A00**

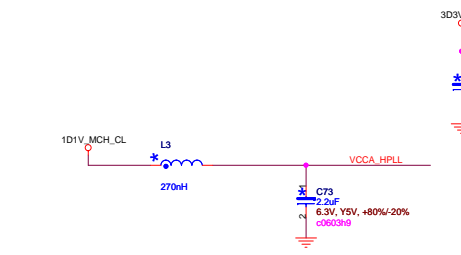
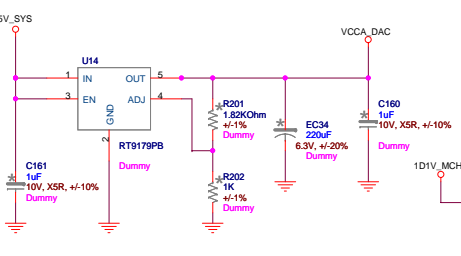
Date: Monday, September 01, 2008 Sheet 12 of 45

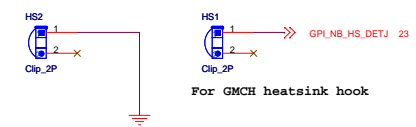
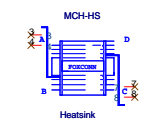
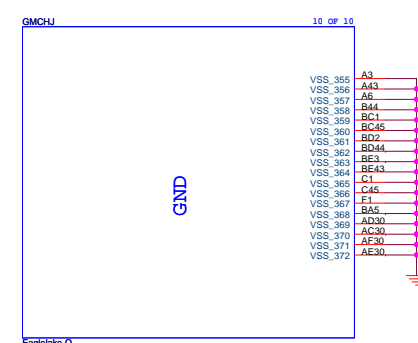
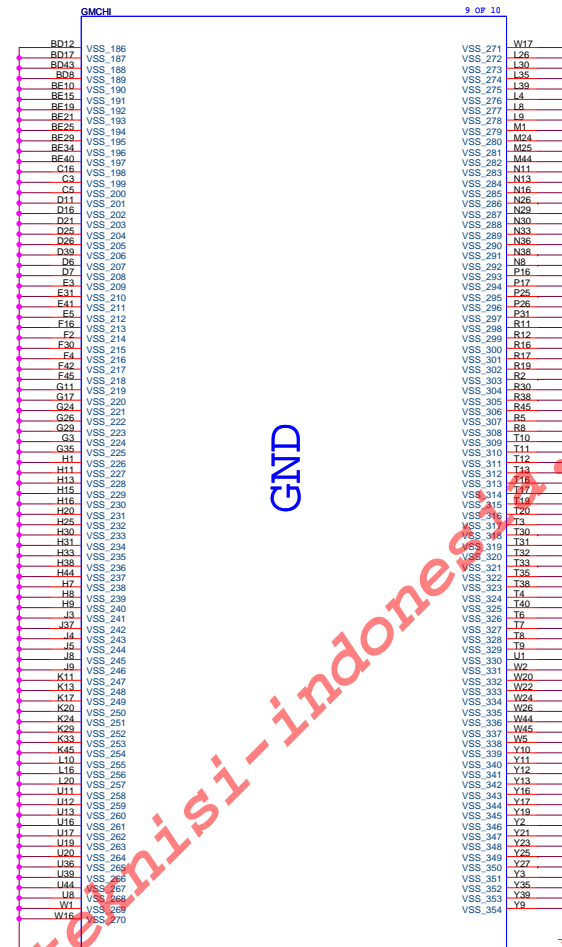
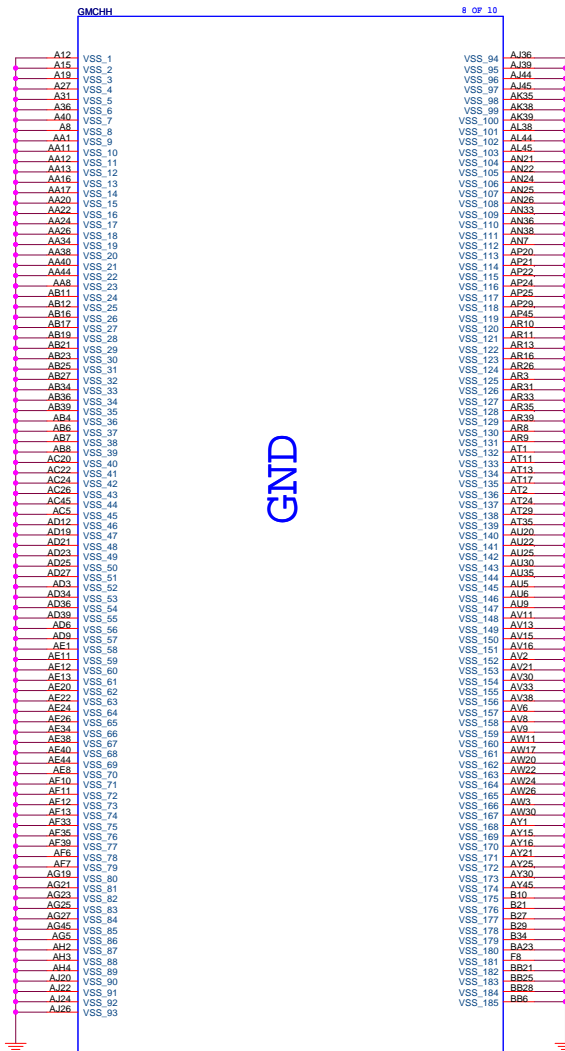


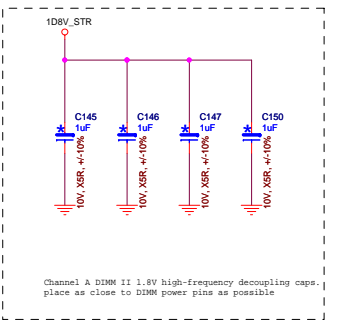
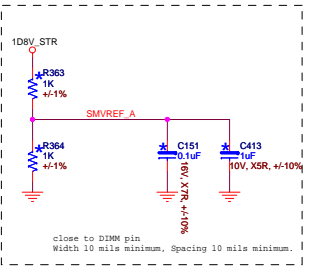
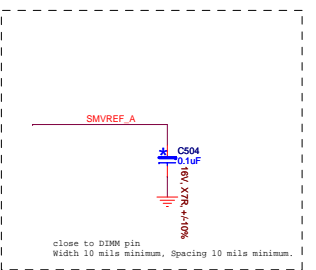
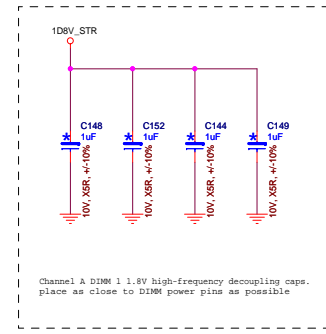
Modify according to Intel MOW50



Stuff for Non-Graphic sku







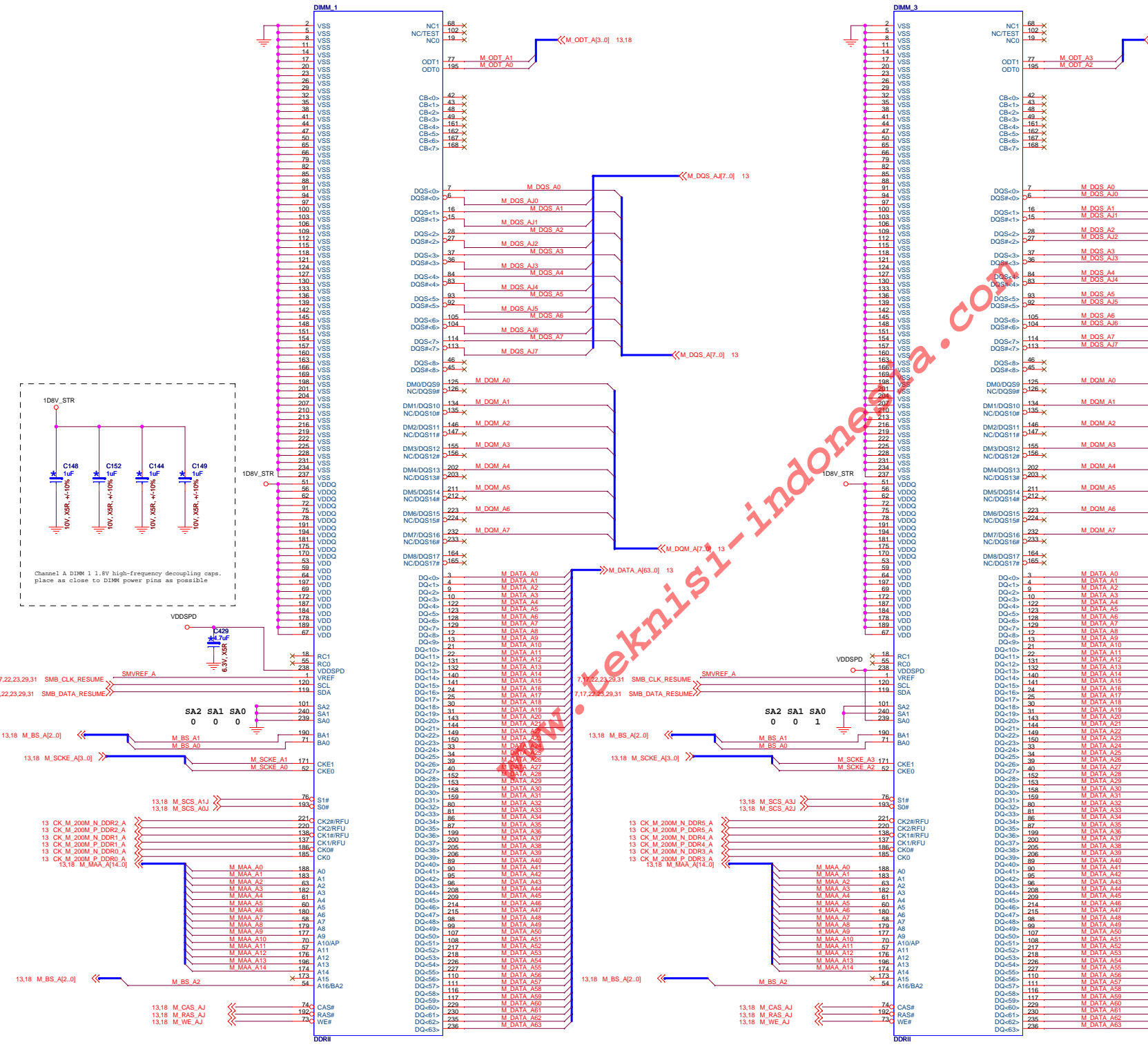
DDR II Channel A DIMM 1, 3

GAO

Rev A00

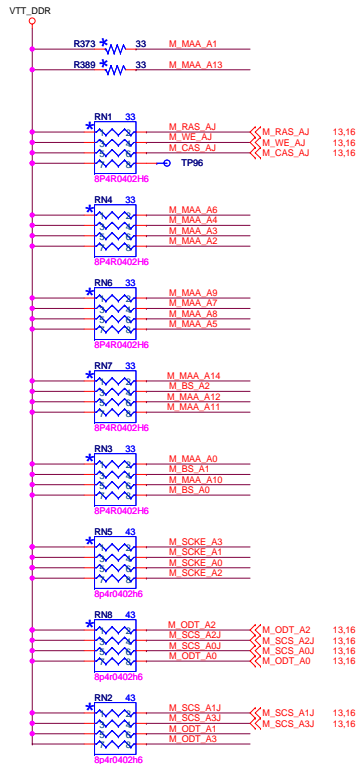
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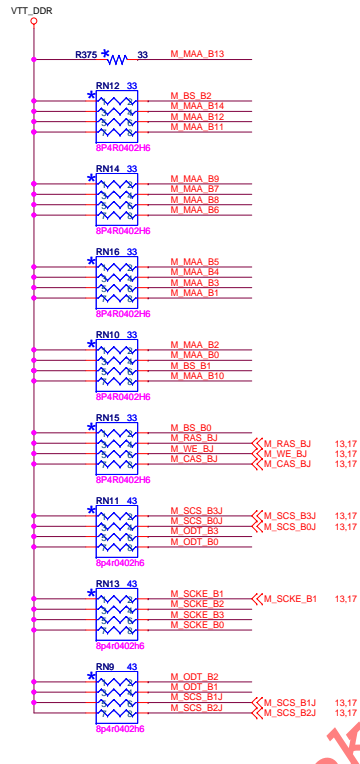


<<M_ODT_A[3..0] 13,16
 <<M_SCKE_A[3..0] 13,16
 <<M_BS_A[2..0] 13,16
 <<M_MAA_A[14..0] 13,16

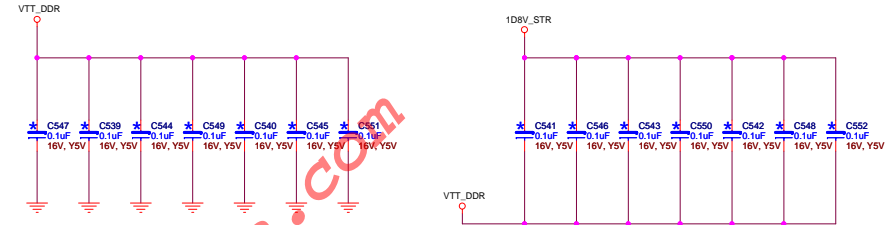
<<M_SCKE_B[3..0] 13,17
 <<M_BS_B[2..0] 13,17
 <<M_MAA_B[14..0] 13,17
 <<M_ODT_B[3..0] 13,17



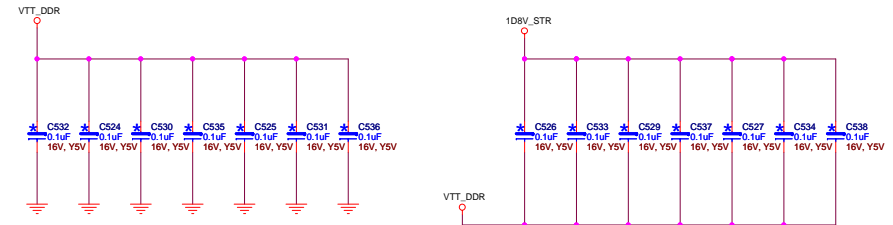
Channel A VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



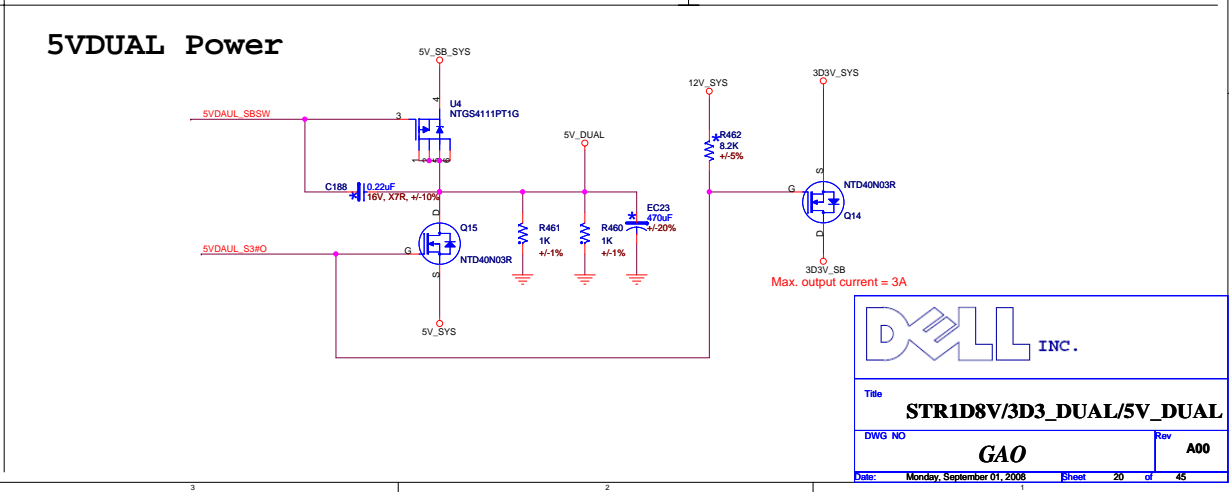
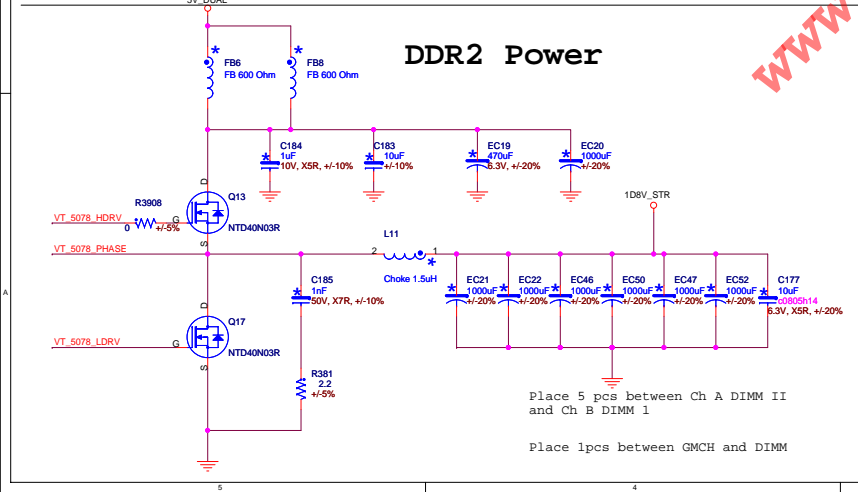
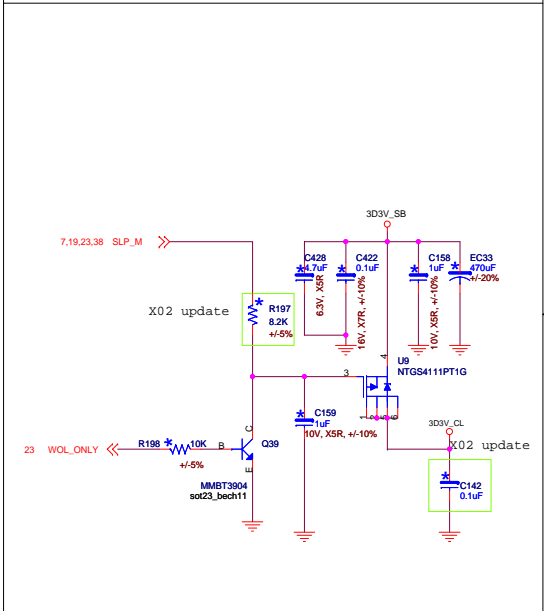
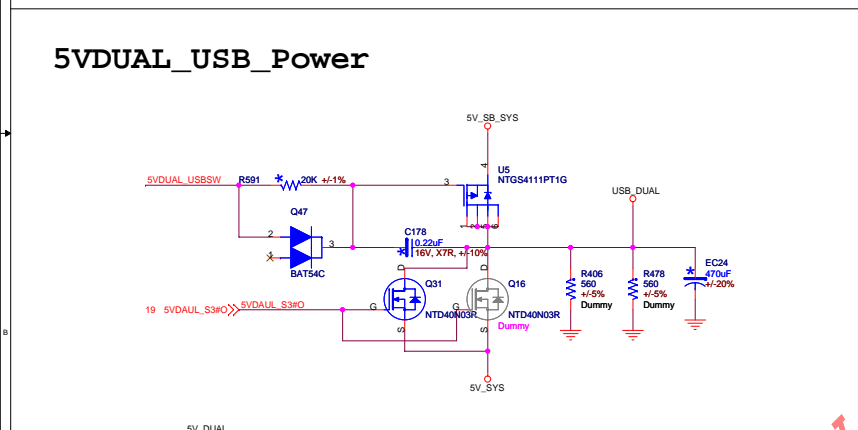
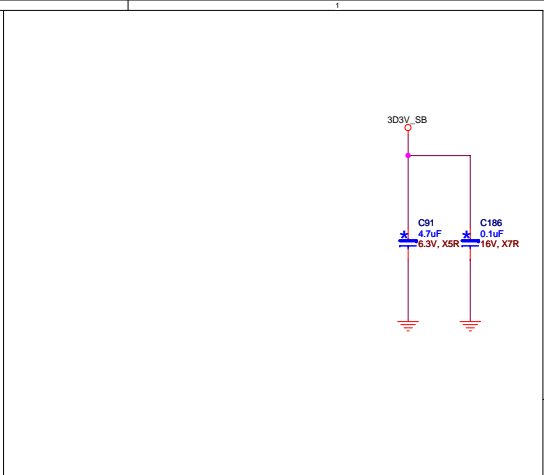
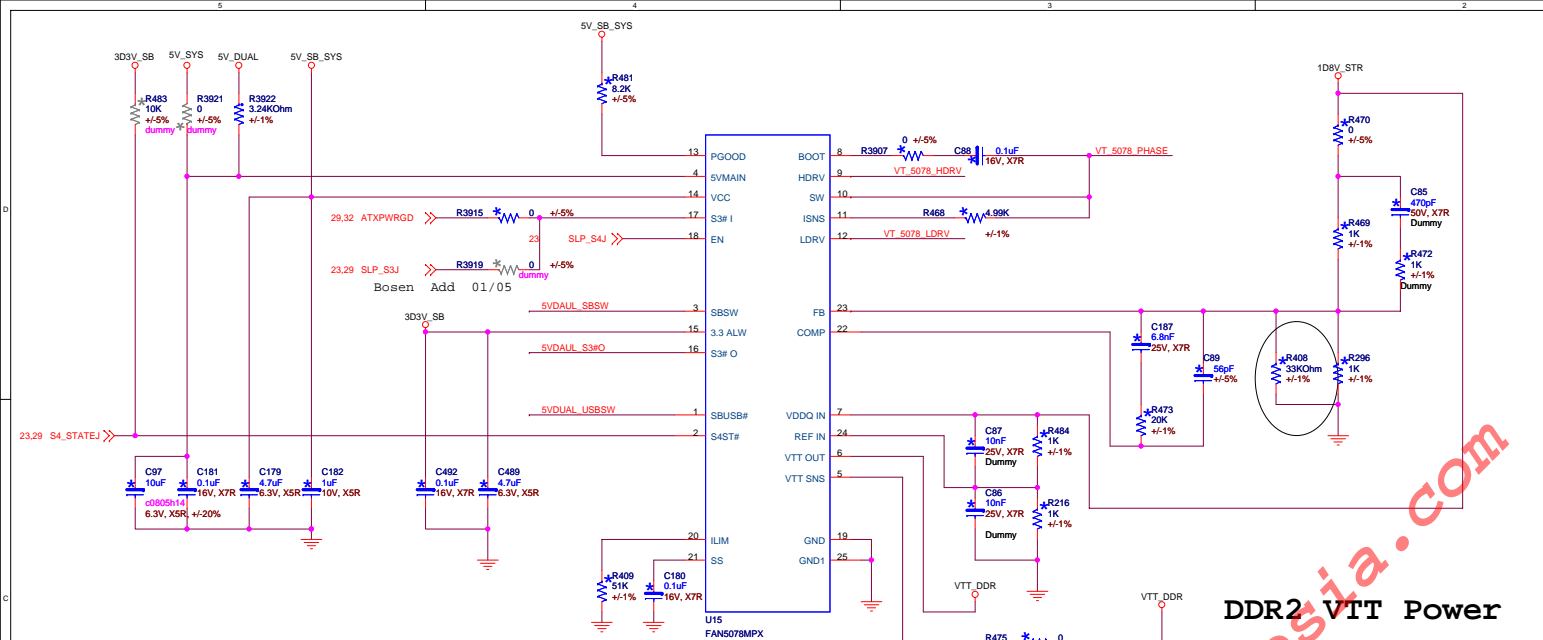
Channel B VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



Channel A VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

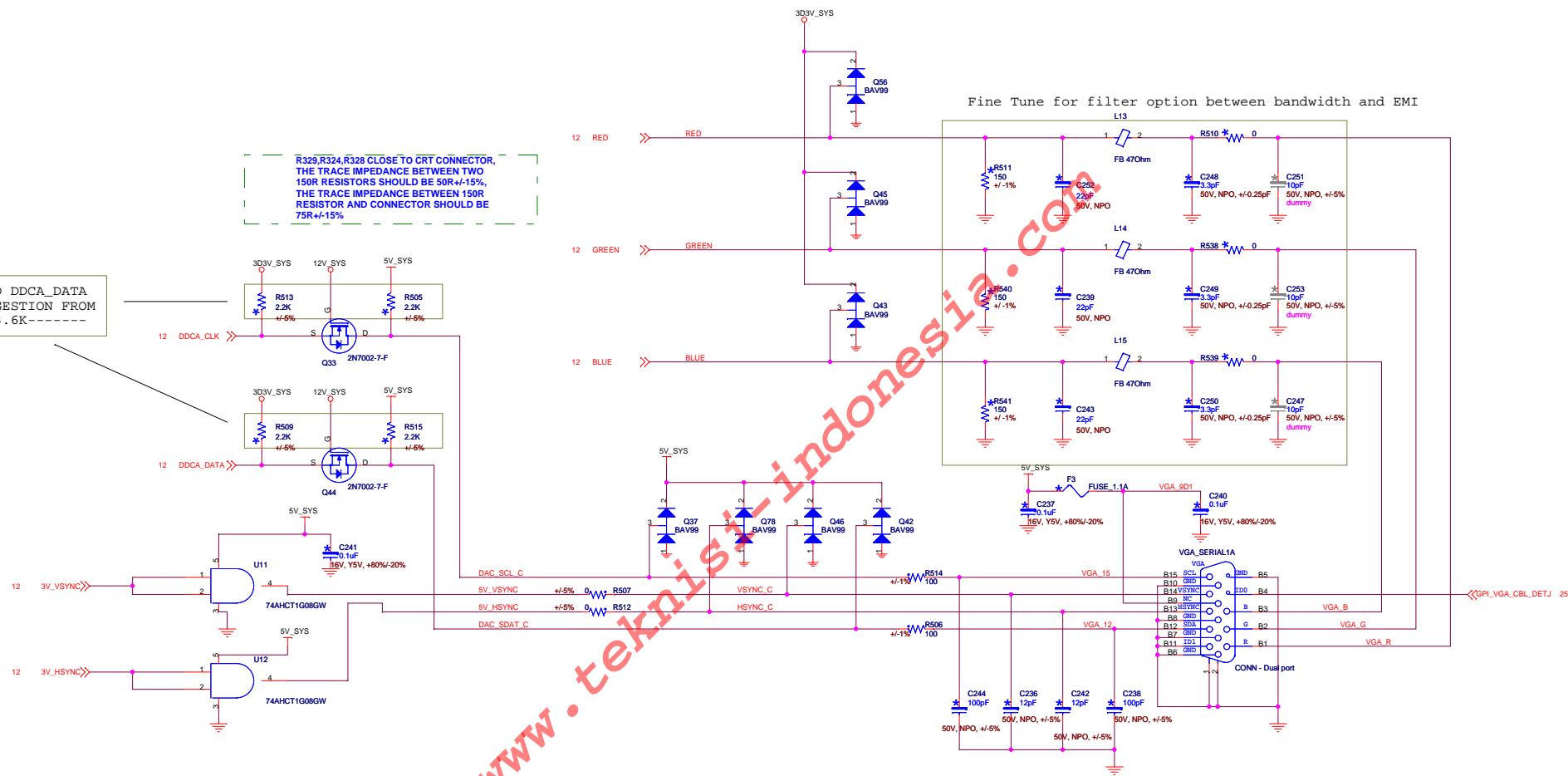


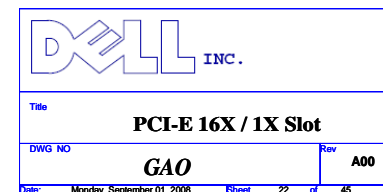
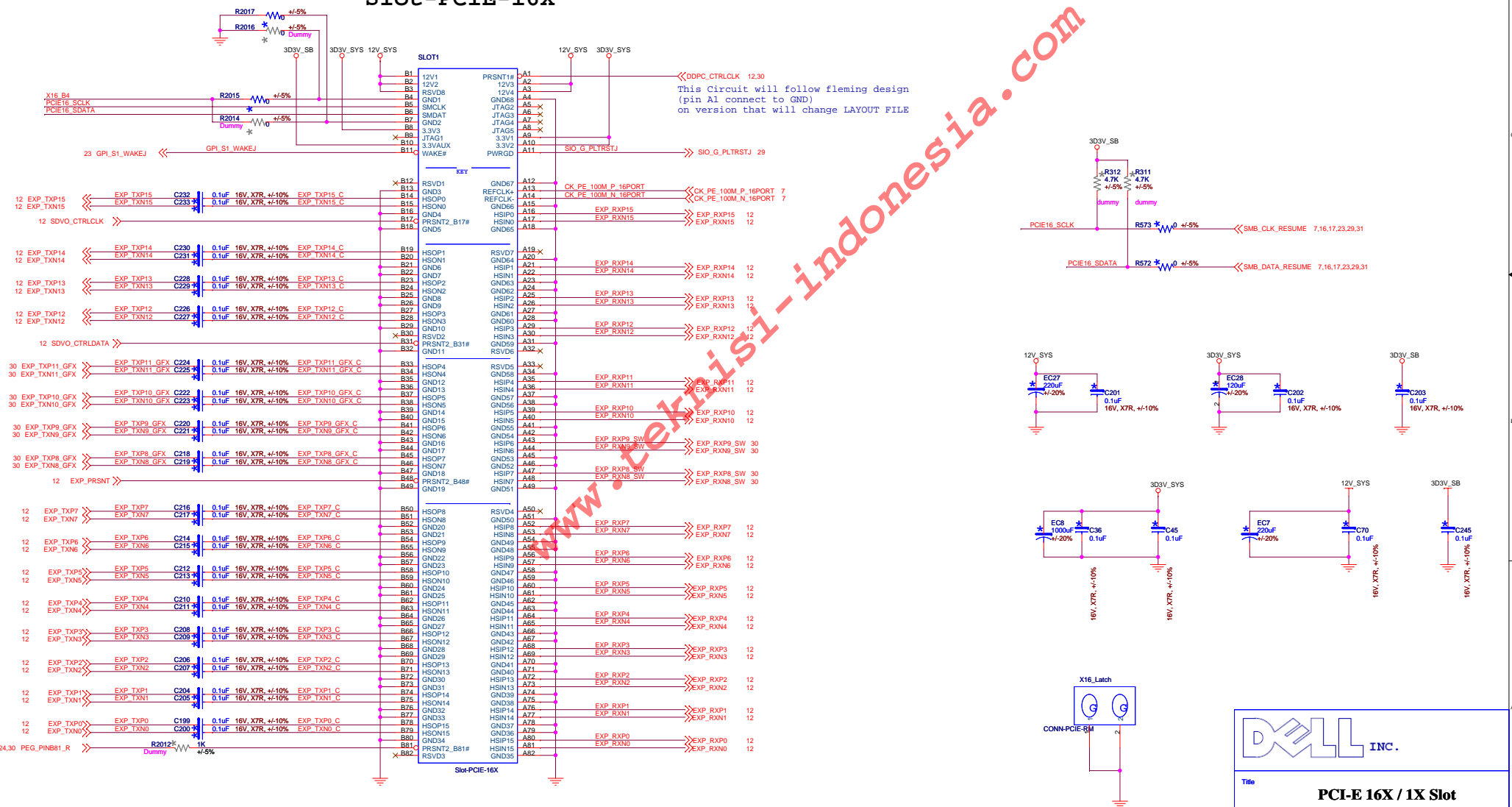
Channel B VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

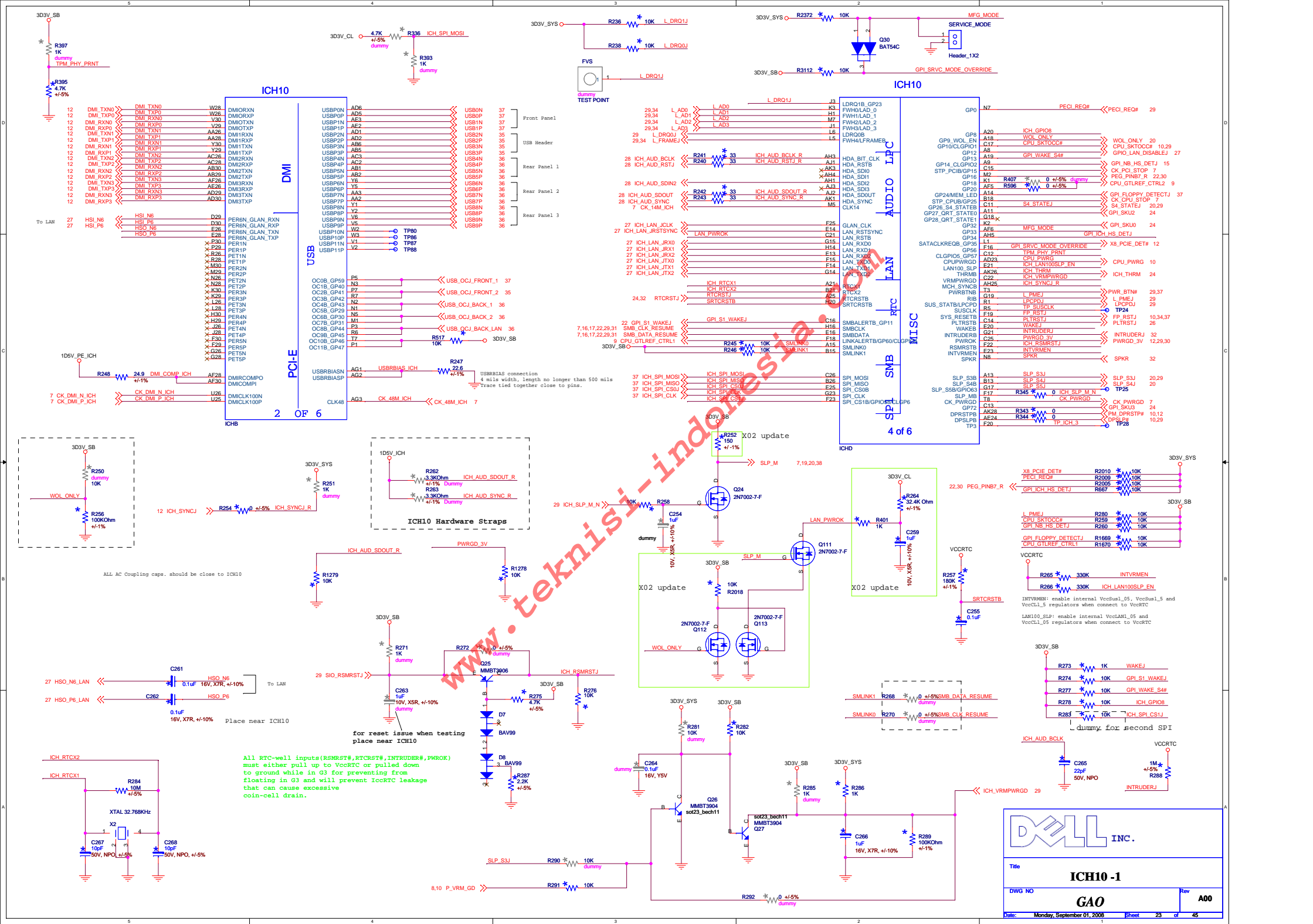


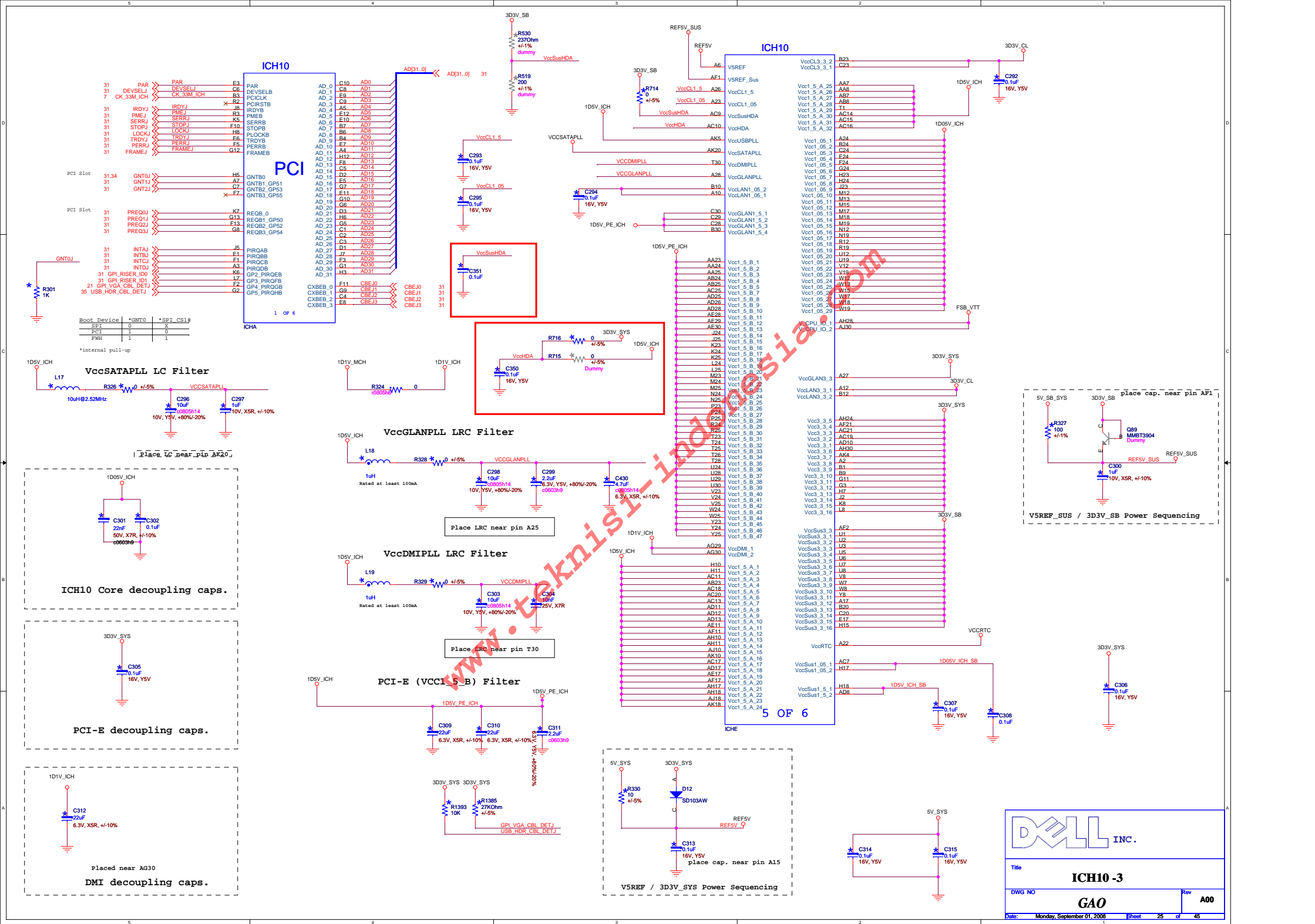
DDCA_CLK AND DDCA_DATA
PULL-UP SUGGESTION FROM
INTEL 2.2K-3.6K-----

R329,R324,R328 CLOSE TO CRT CONNECTOR,
THE TRACE IMPEDANCE BETWEEN TWO
150R RESISTORS SHOULD BE 50R +/-15%,
THE TRACE IMPEDANCE BETWEEN 150R
RESISTOR AND CONNECTOR SHOULD BE
75R +/-15%



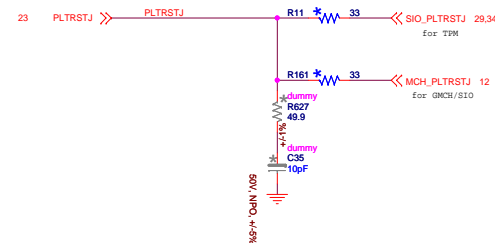
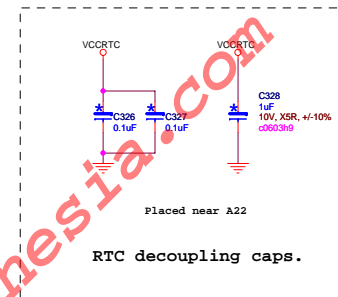
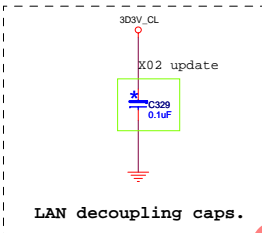
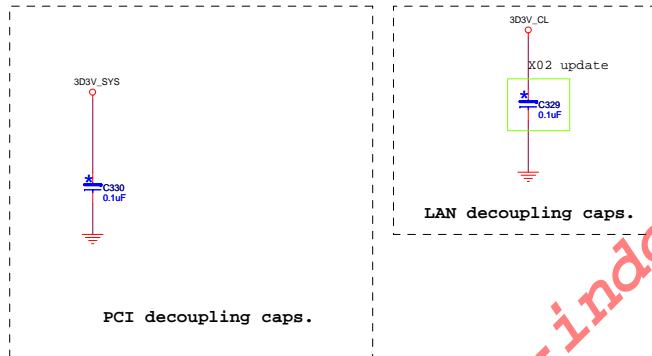
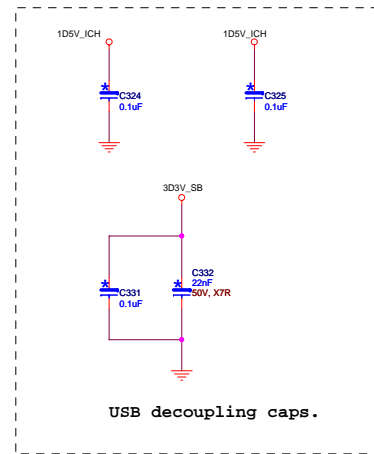
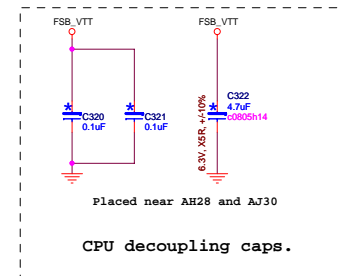
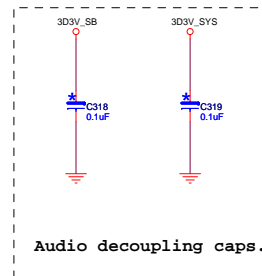
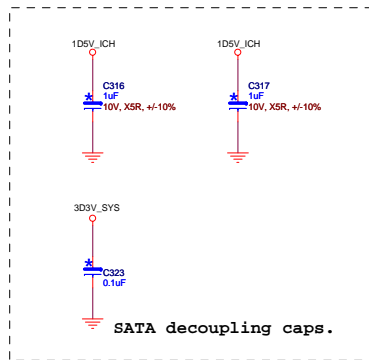
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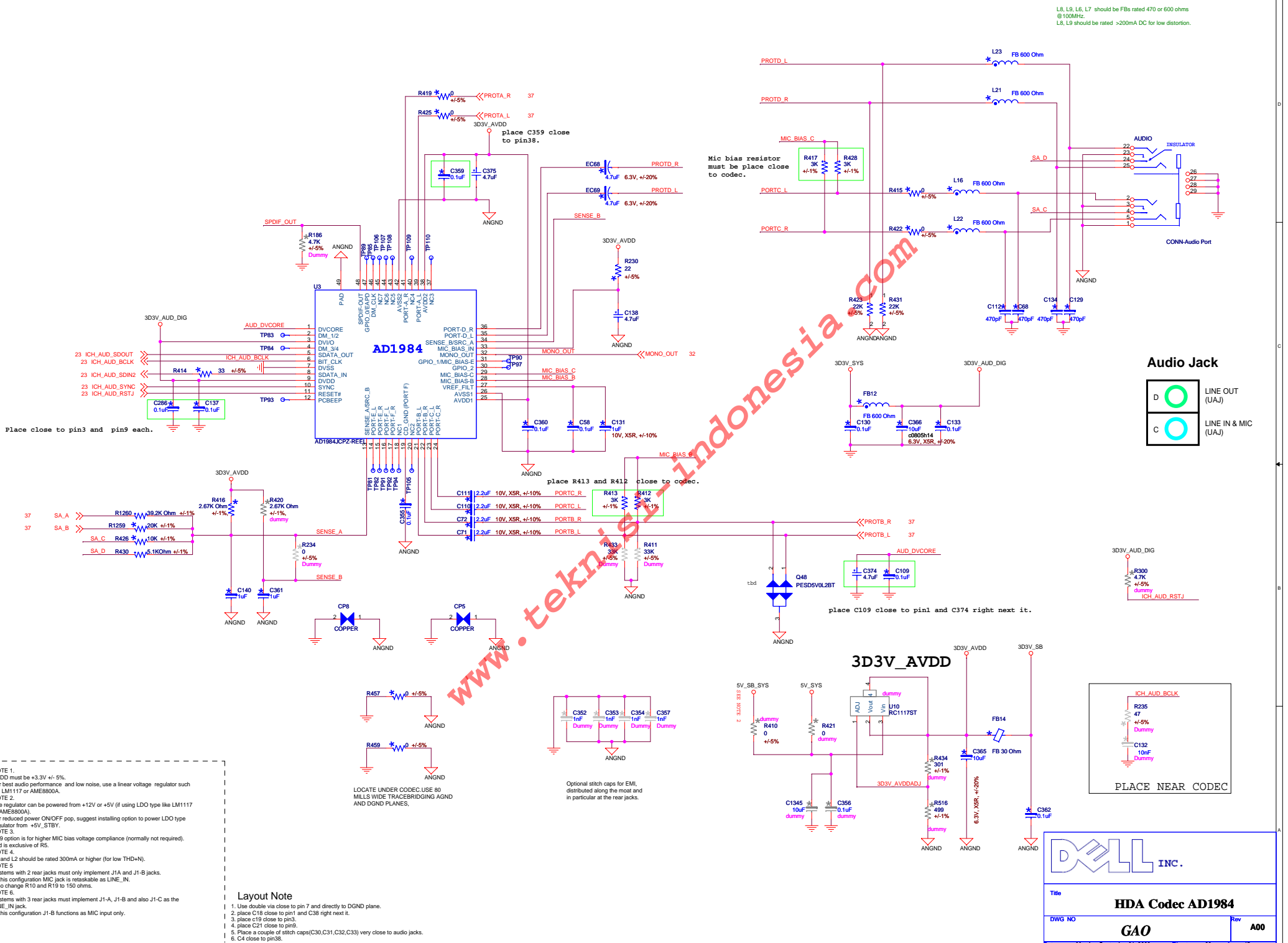


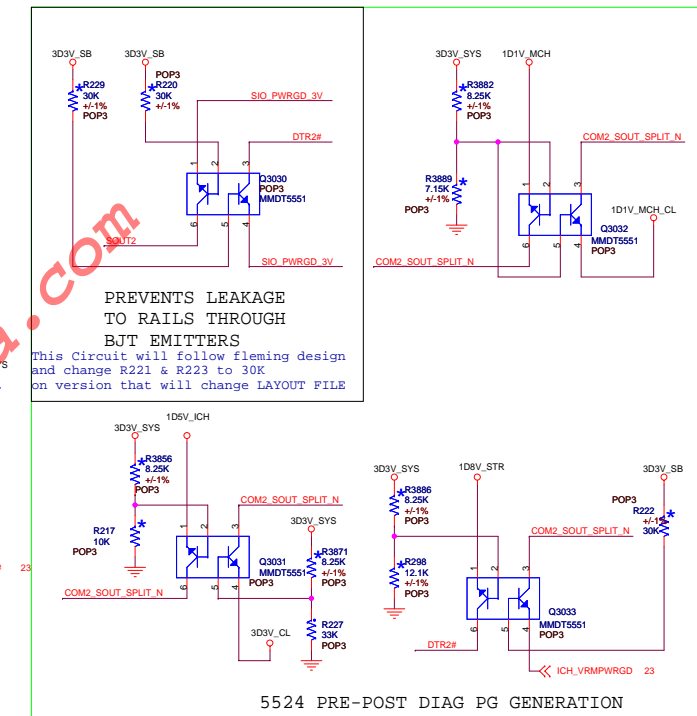
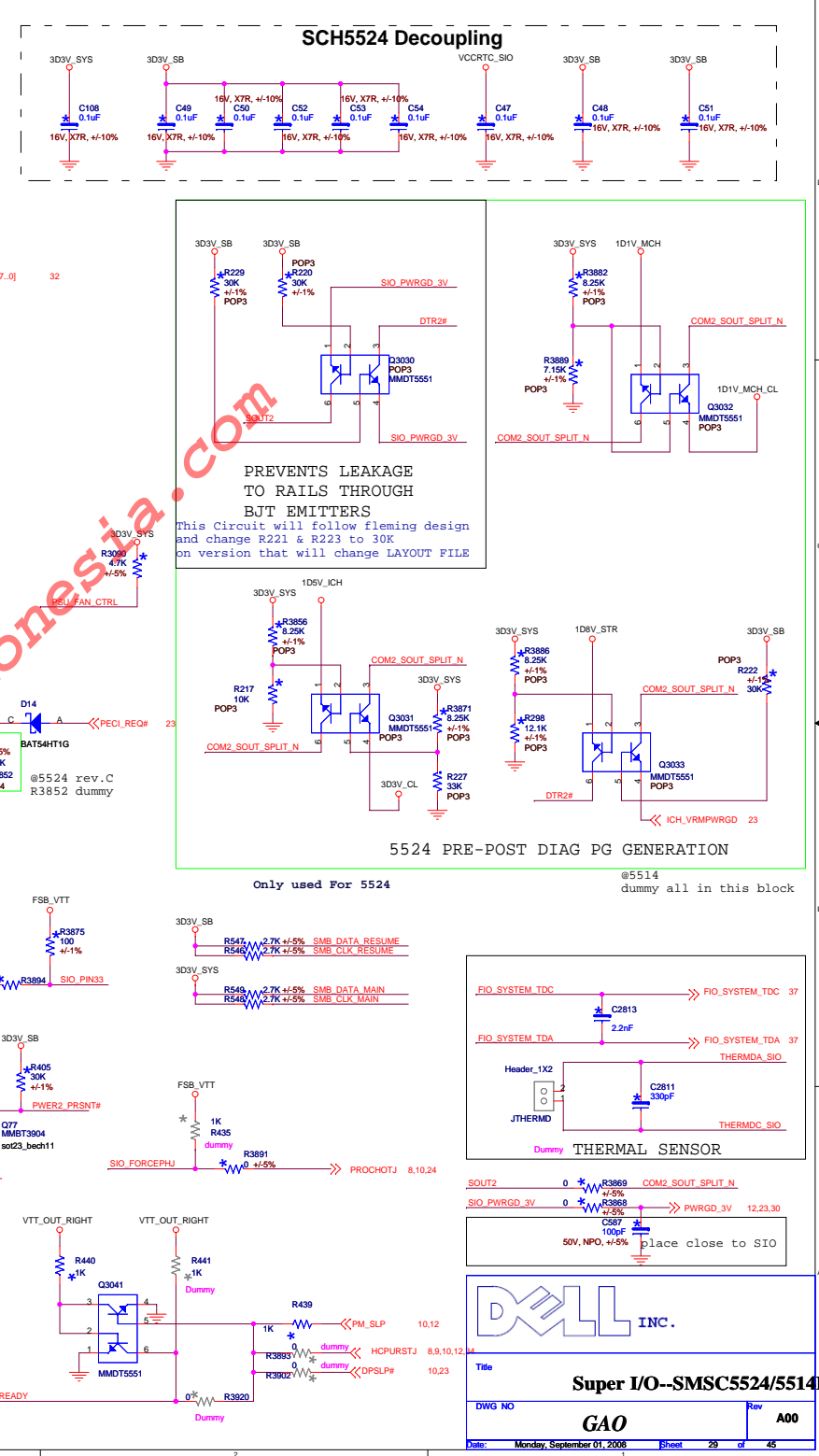
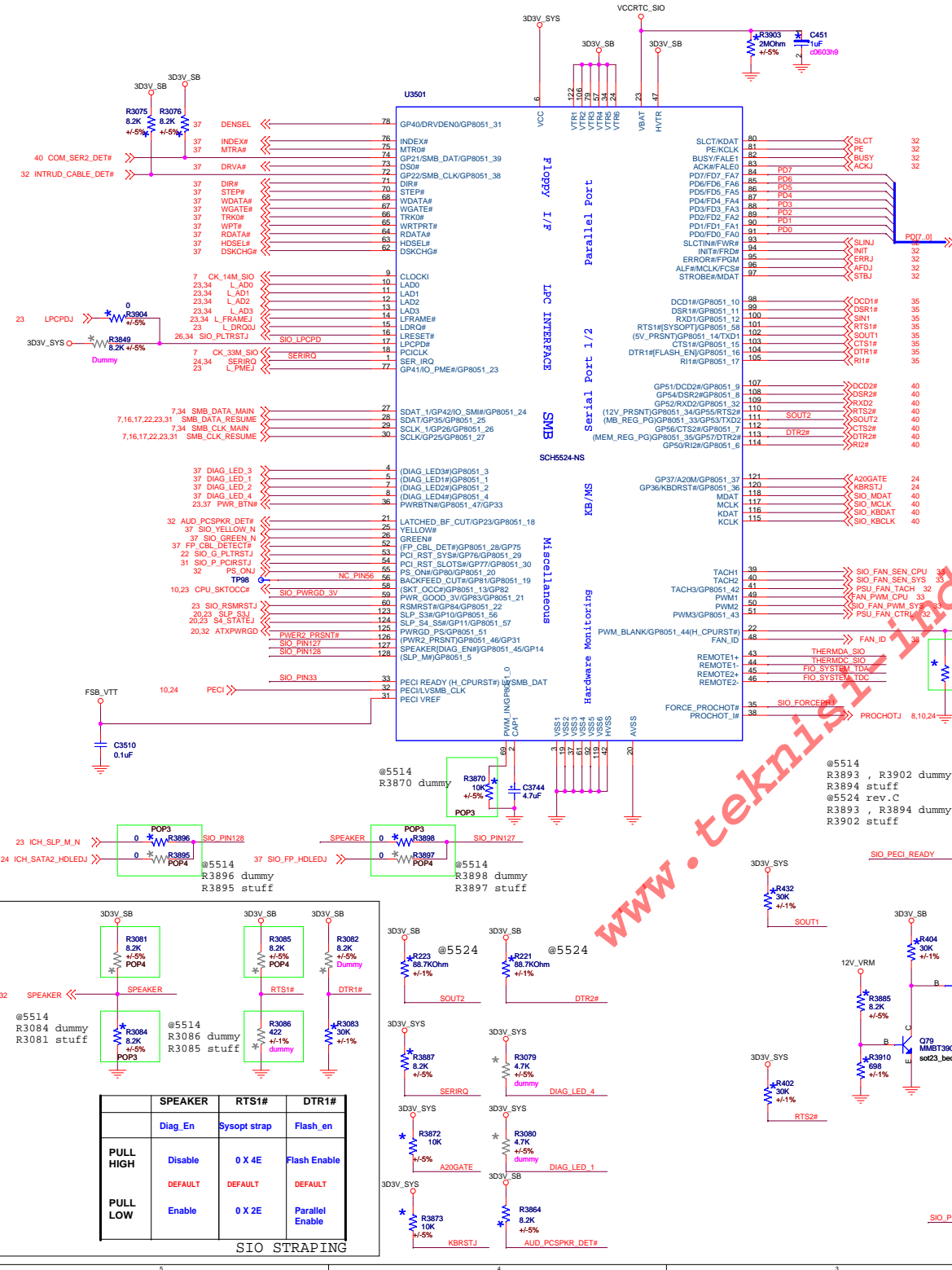


ICH10		
G30	VSS_100	VSS_099
G29	VSS_101	VSS_098
G25	VSS_102	VSS_097
F9	VSS_103	VSS_096
F6	VSS_104	VSS_095
F28	VSS_105	VSS_094
F26	VSS_106	VSS_093
F21	VSS_107	VSS_092
E30	VSS_108	VSS_091
E29	VSS_109	VSS_090
E22	VSS_110	VSS_089
E2	VSS_111	VSS_088
E18	VSS_112	VSS_087
D28	VSS_113	VSS_086
D25	VSS_114	VSS_085
D22	VSS_115	VSS_084
D2	VSS_116	VSS_083
B8	VSS_117	VSS_082
B5	VSS_118	VSS_081
B28	VSS_119	VSS_080
B25	VSS_120	VSS_079
B2	VSS_121	VSS_078
B17	VSS_122	VSS_077
B19	VSS_123	VSS_076
B14	VSS_124	VSS_075
B11	VSS_125	VSS_074
AK9	VSS_126	VSS_073
AK30	VSS_127	VSS_072
AK29	VSS_128	VSS_071
AK2	VSS_129	VSS_070
AK16	VSS_130	VSS_069
AK14	VSS_131	VSS_068
AK12	VSS_132	VSS_067
AJ8	VSS_133	VSS_066
AJ6	VSS_134	VSS_065
AJ5	VSS_135	VSS_064
AJ23	VSS_136	VSS_063
AJ20	VSS_137	VSS_062
AJ16	VSS_138	VSS_061
AJ14	VSS_139	VSS_060
AJ12	VSS_140	VSS_059
AH8	VSS_141	VSS_058
AH6	VSS_142	VSS_057
AH20	VSS_143	VSS_056
AH2	VSS_144	VSS_055
AH19	VSS_145	VSS_054
AH15	VSS_146	VSS_053
AH13	VSS_147	VSS_052
AG28	VSS_148	VSS_051
AF9	VSS_149	VSS_050
AF7	VSS_150	VSS_049
AF29	VSS_151	VSS_048
AF25	VSS_152	VSS_047
AF23	VSS_153	VSS_046
AF20	VSS_154	VSS_045
AF15	VSS_155	VSS_044
AF13	VSS_156	VSS_043
AE9	VSS_157	VSS_042
AE8	VSS_158	VSS_041
AE6	VSS_159	VSS_040
AE5	VSS_160	VSS_039
AE25	VSS_161	VSS_038
AE19	VSS_162	VSS_037
AE16	VSS_163	VSS_036
AE18	VSS_164	VSS_035
AE15	VSS_165	VSS_034
AE14	VSS_166	VSS_033
AE12	VSS_167	VSS_032
AE10	VSS_168	VSS_031
AE1	VSS_169	VSS_030
AD7	VSS_170	VSS_029
AD3	VSS_171	VSS_028
AD22	VSS_172	VSS_027
AD19	VSS_173	VSS_026
AD18	VSS_174	VSS_025
AD16	VSS_175	VSS_024
AD15	VSS_176	VSS_023
AD14	VSS_177	VSS_022
AC8	VSS_178	VSS_021
AC6	VSS_179	VSS_020
AC5	VSS_180	VSS_019
AC30	VSS_181	VSS_018
AC29	VSS_182	VSS_017
AC24	VSS_183	VSS_016
AC12	VSS_184	VSS_015
AC1	VSS_185	VSS_014
AB3	VSS_186	VSS_013
AB28	VSS_187	VSS_012
AB25	VSS_188	VSS_011
AB2	VSS_189	VSS_010
AA6	VSS_190	VSS_009
AA5	VSS_191	VSS_008
	VSS_192	VSS_007
	VSS_193	VSS_006
AK27	VSS_194	VSS_004
AK20	VSS_195	VSS_003
AJ4	VSS_196	VSS_002
AF3	VSS_197	VSS_001
B27	VSS_198	

ICH10
6 OF 6

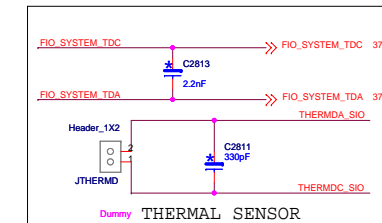






	SPEAKER	RTS1#	DTR1#
	Diag_En	Sysopt strap	Flash_en
PULL HIGH	Disable	0 X 4E	Flash Enable
DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	Enable	0 X 2E	Parallel Enable

SIO STRAPPING



Super I/O--SMSC5524/5514E

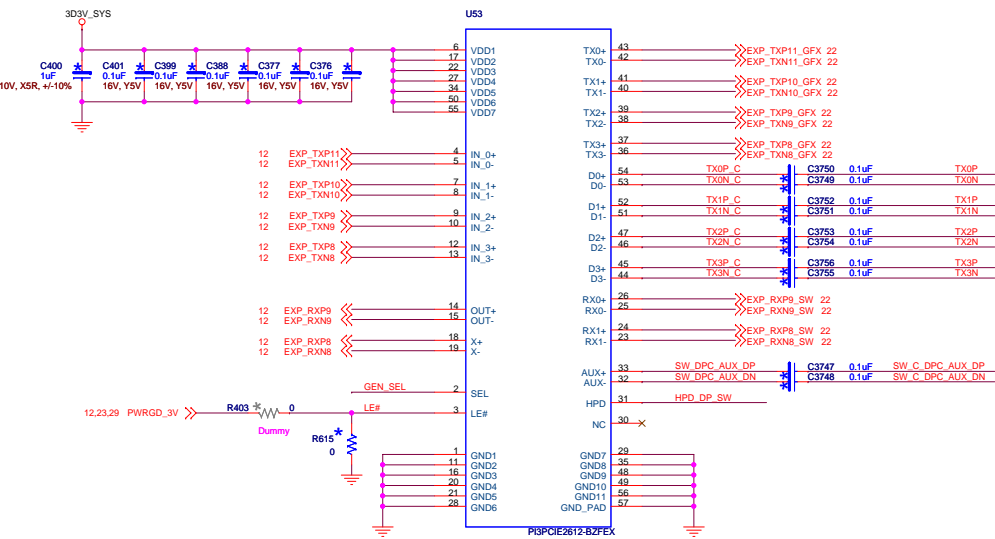
GAO

A00

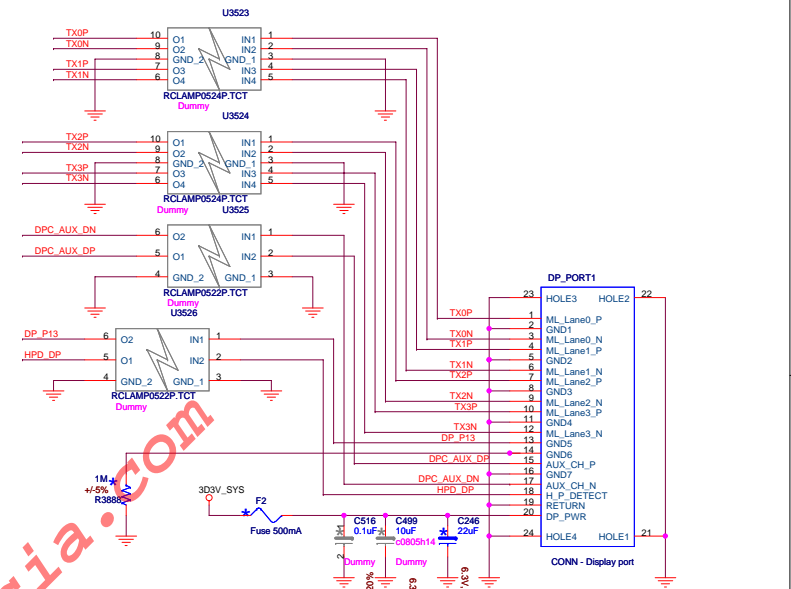
Monday, September 01, 2008

Sheet 29 of 45

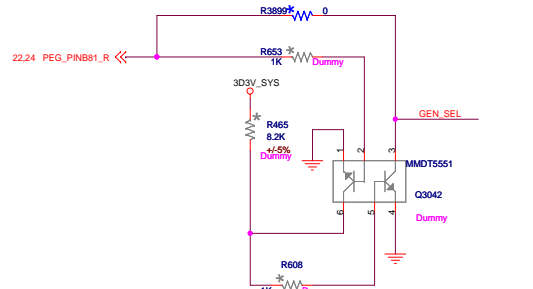
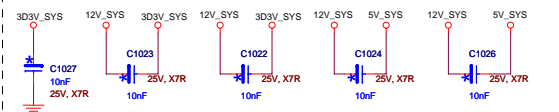
GENII SWITCH



DISPLAY PORT

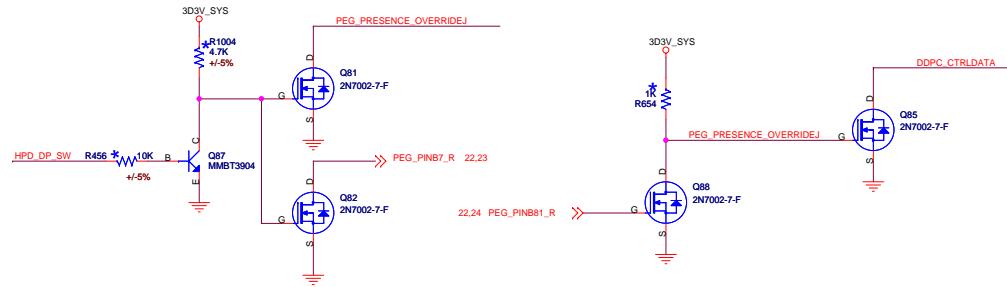
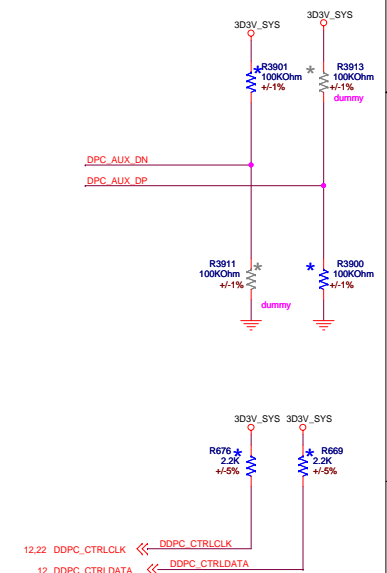
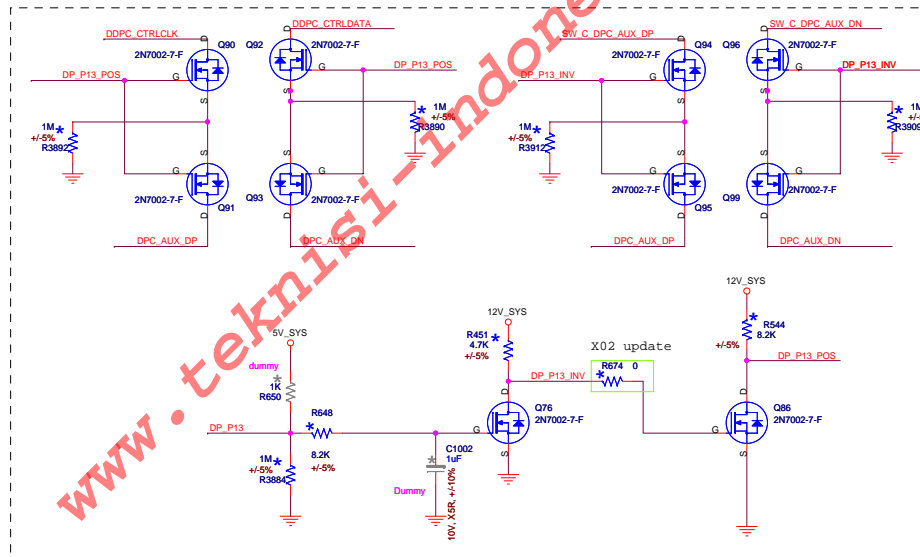
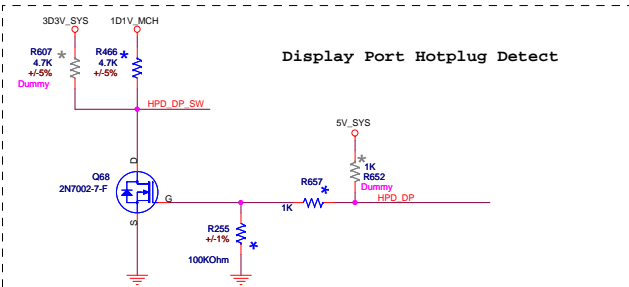


Stitching Cap For DP

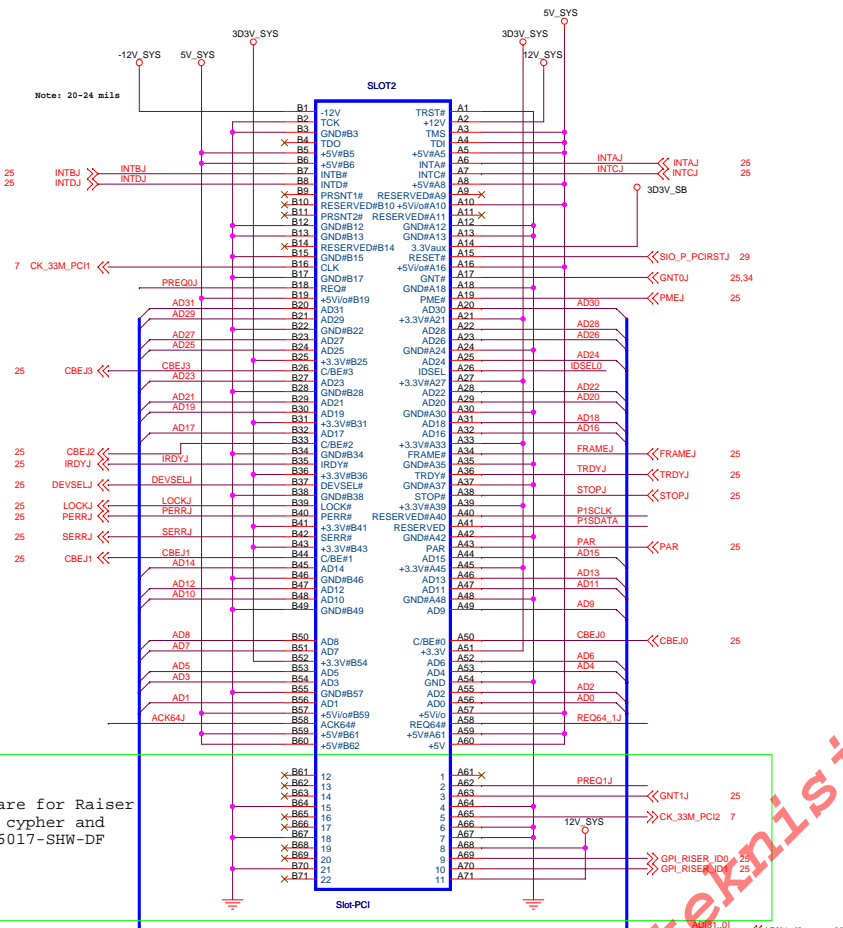


Stuff R3899 and un-pop the buffer circuit

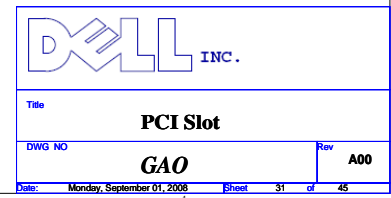
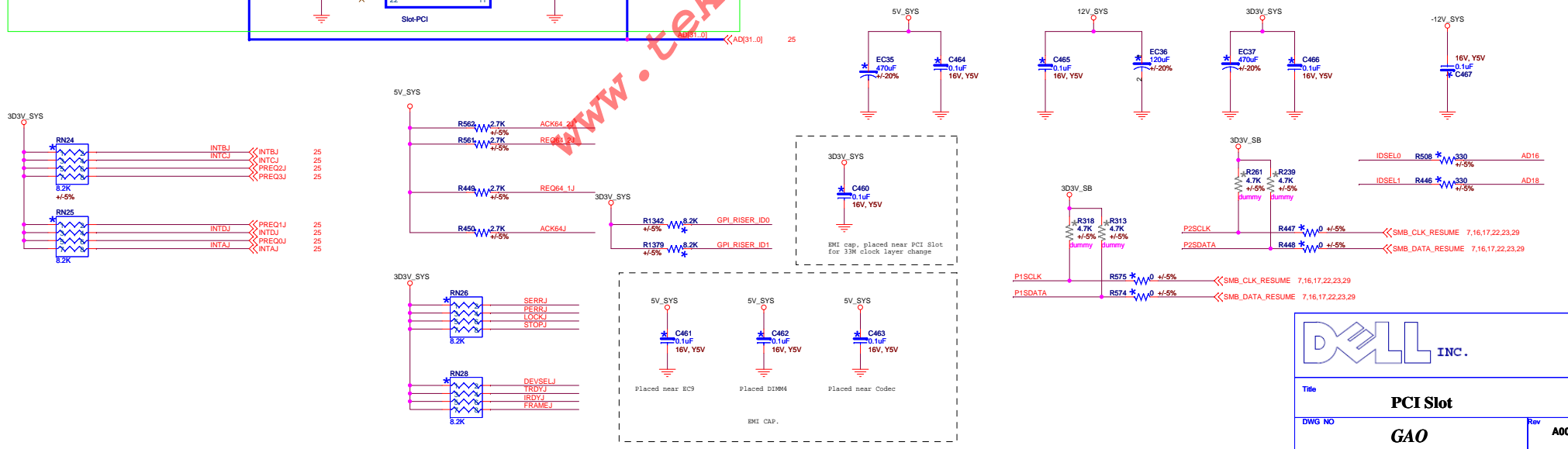
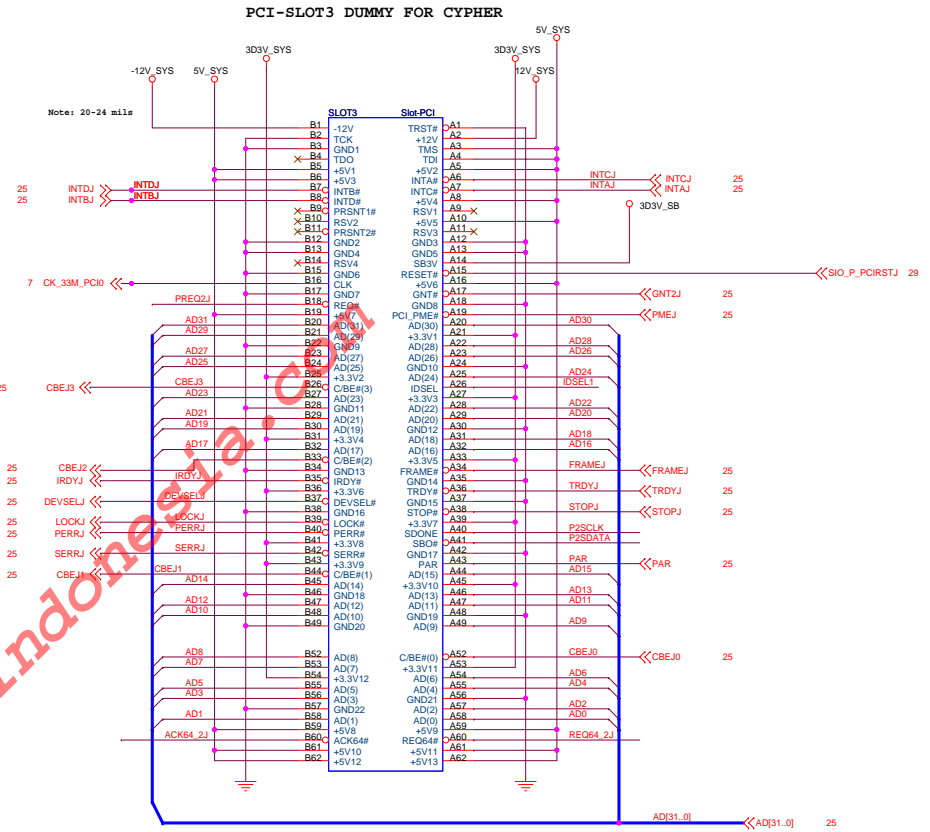
Display Port Hotplug Detect

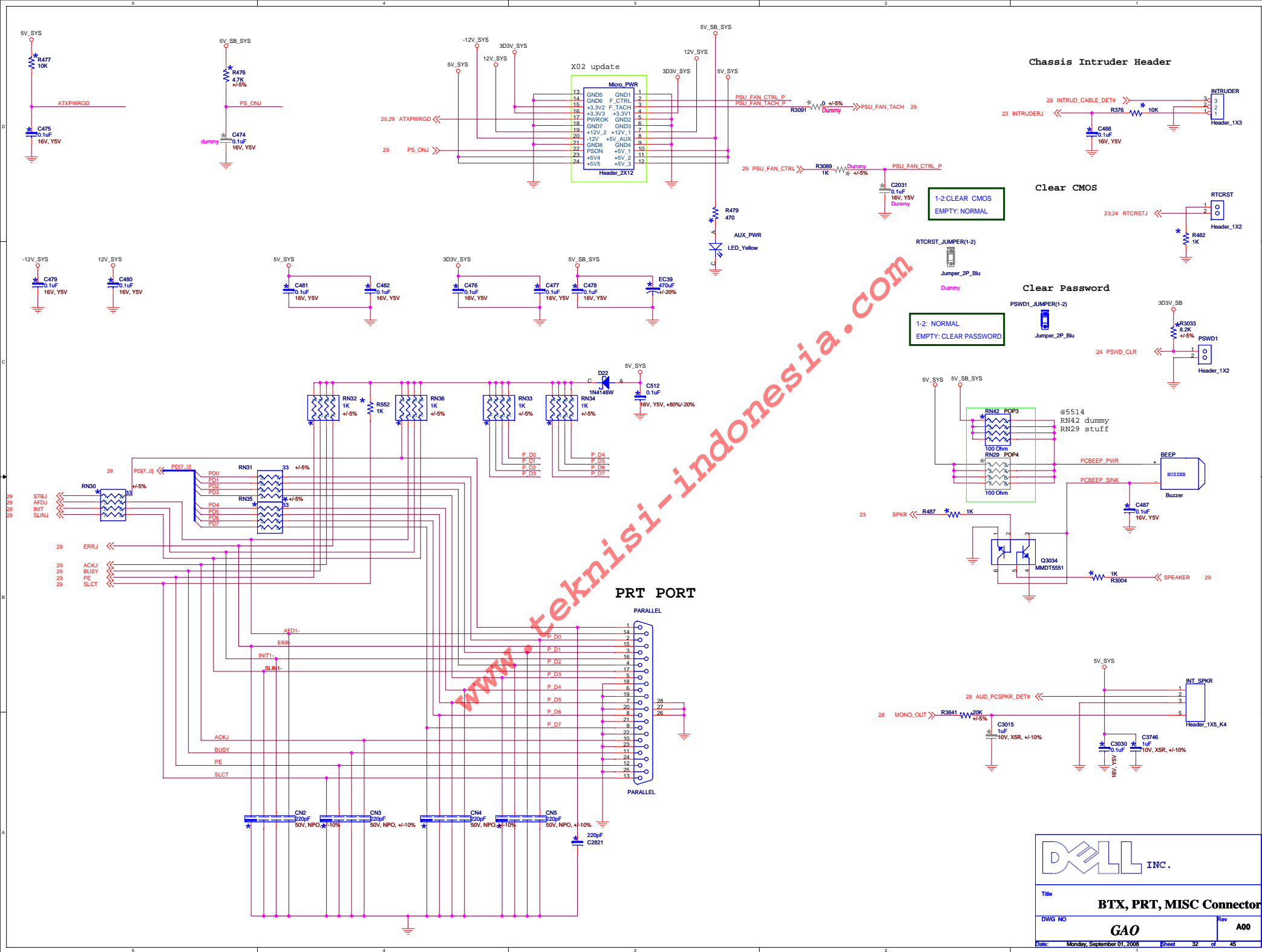


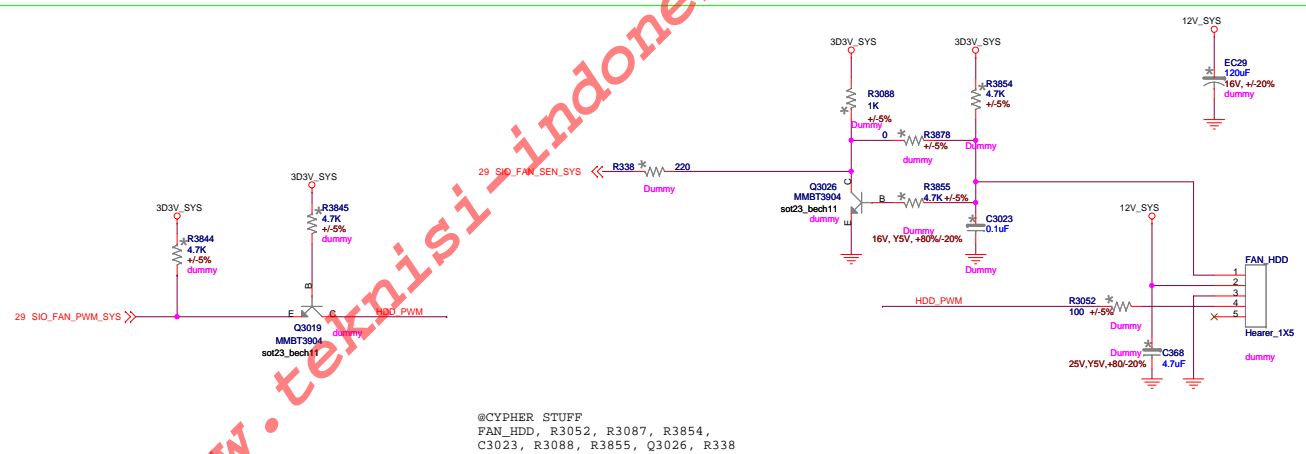
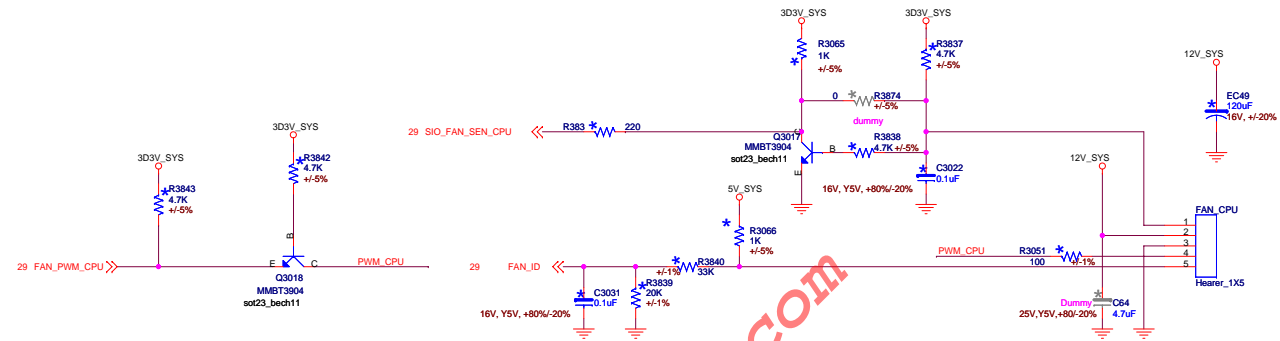
PCI SLOT W/ RISER ONLY FOR NEO
PCI SLOT W/O RISER FOR SMITH & CYPHER



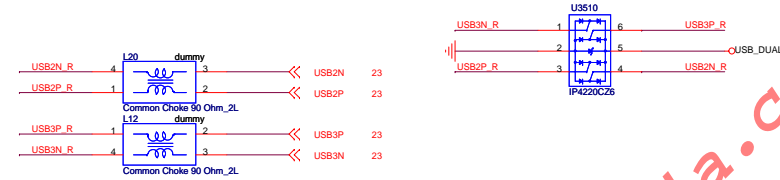
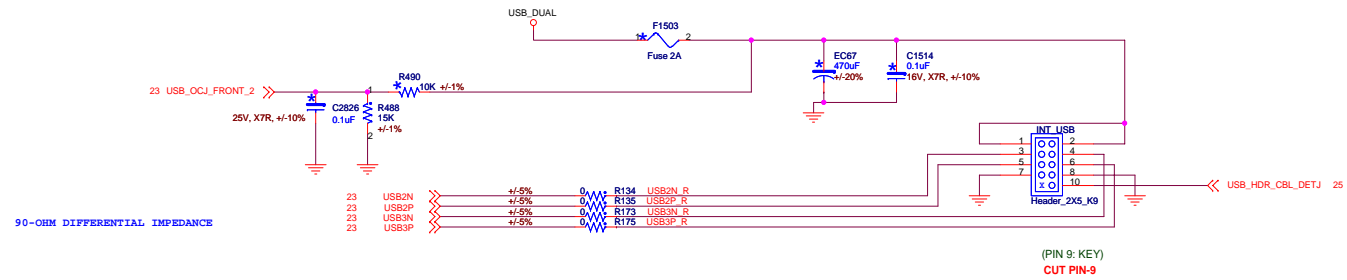
Pin 61 to Pin 71 are for Raiser card for Neo. For cypher and Smith BOM Use EH06017-SHW-DF for Slot2



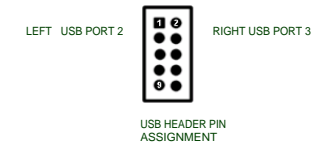




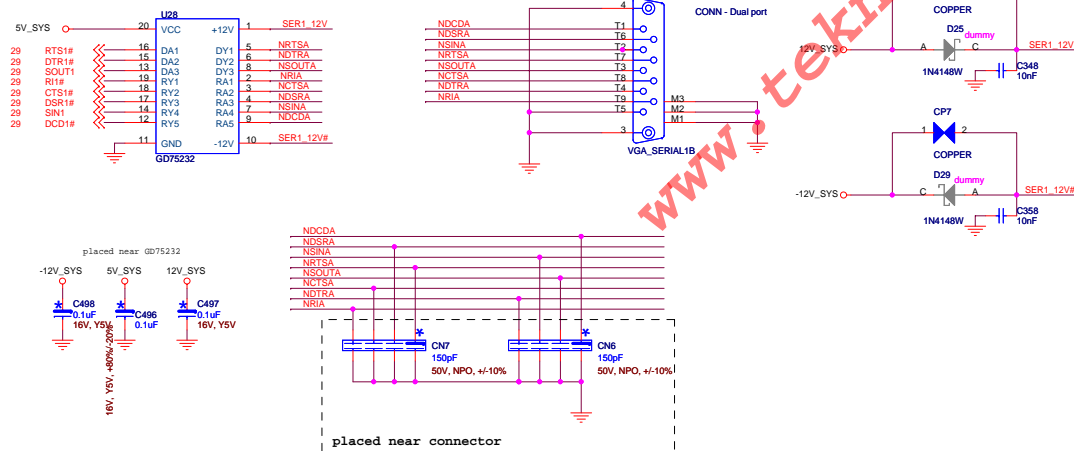
USB



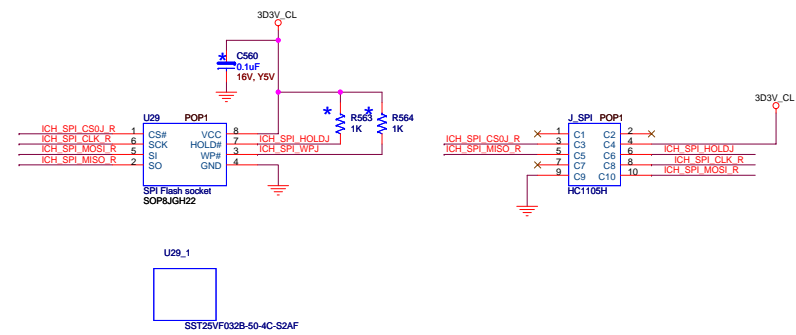
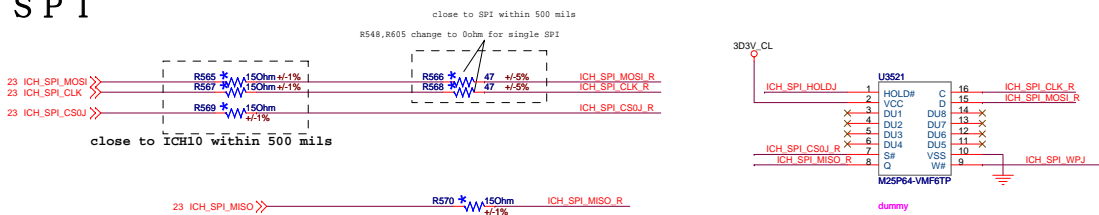
CO-LAY with Four 0603 Serial Resistors



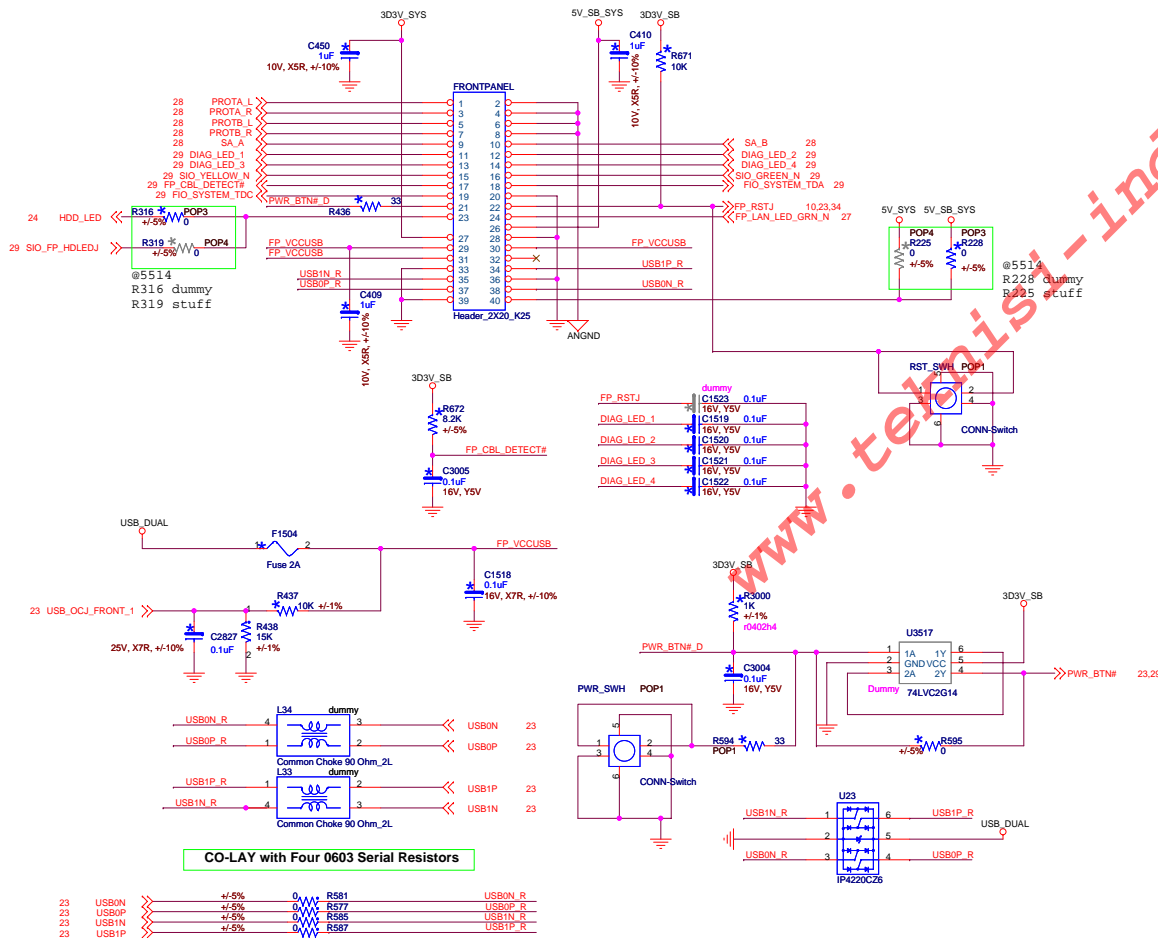
COM 1



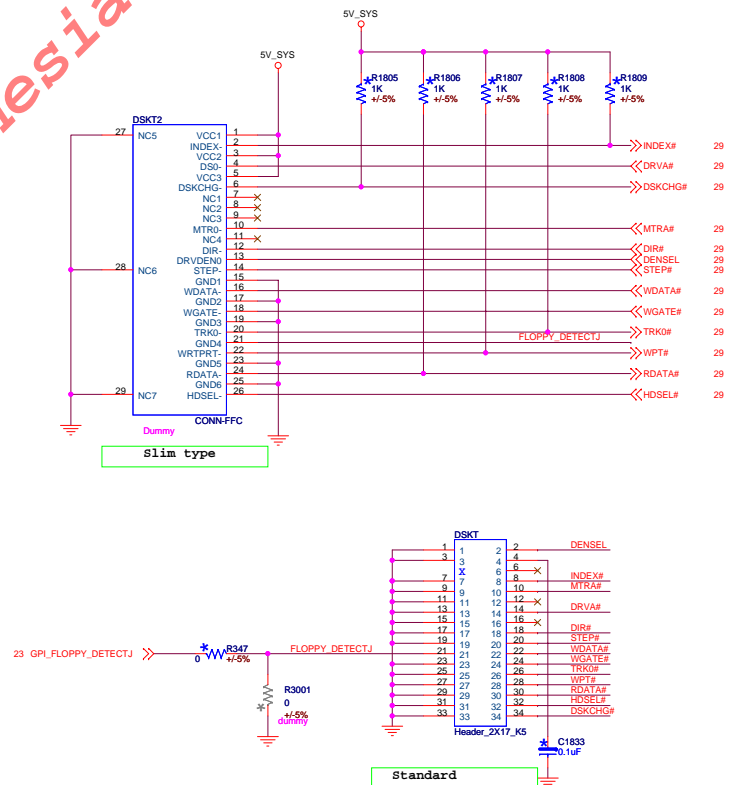
S P I



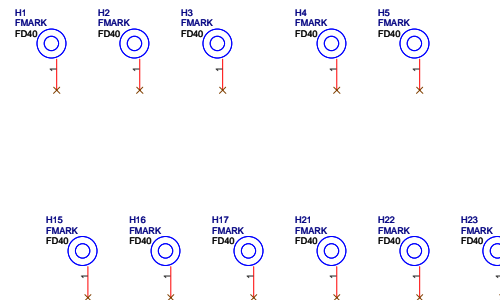
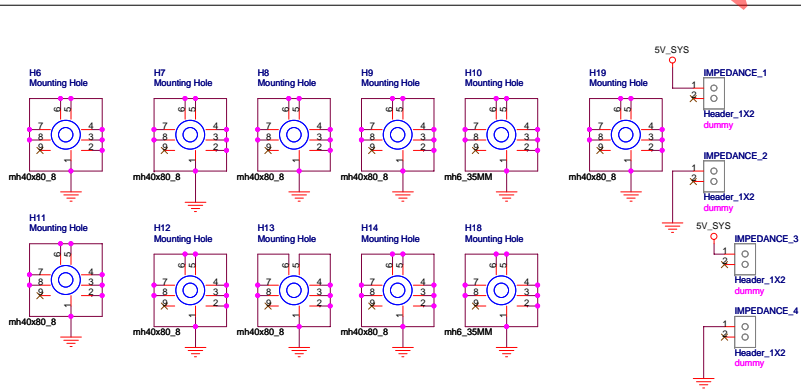
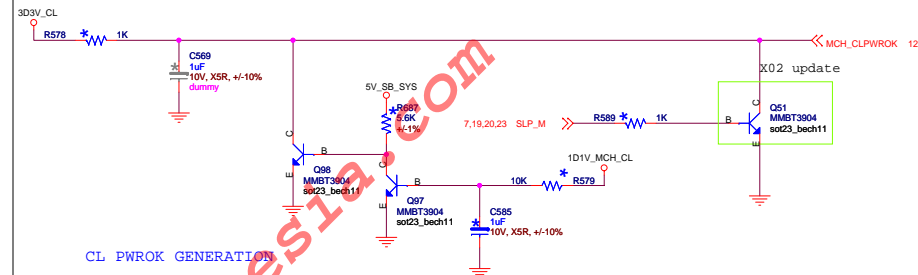
FRONT PANEL



FLOPPY

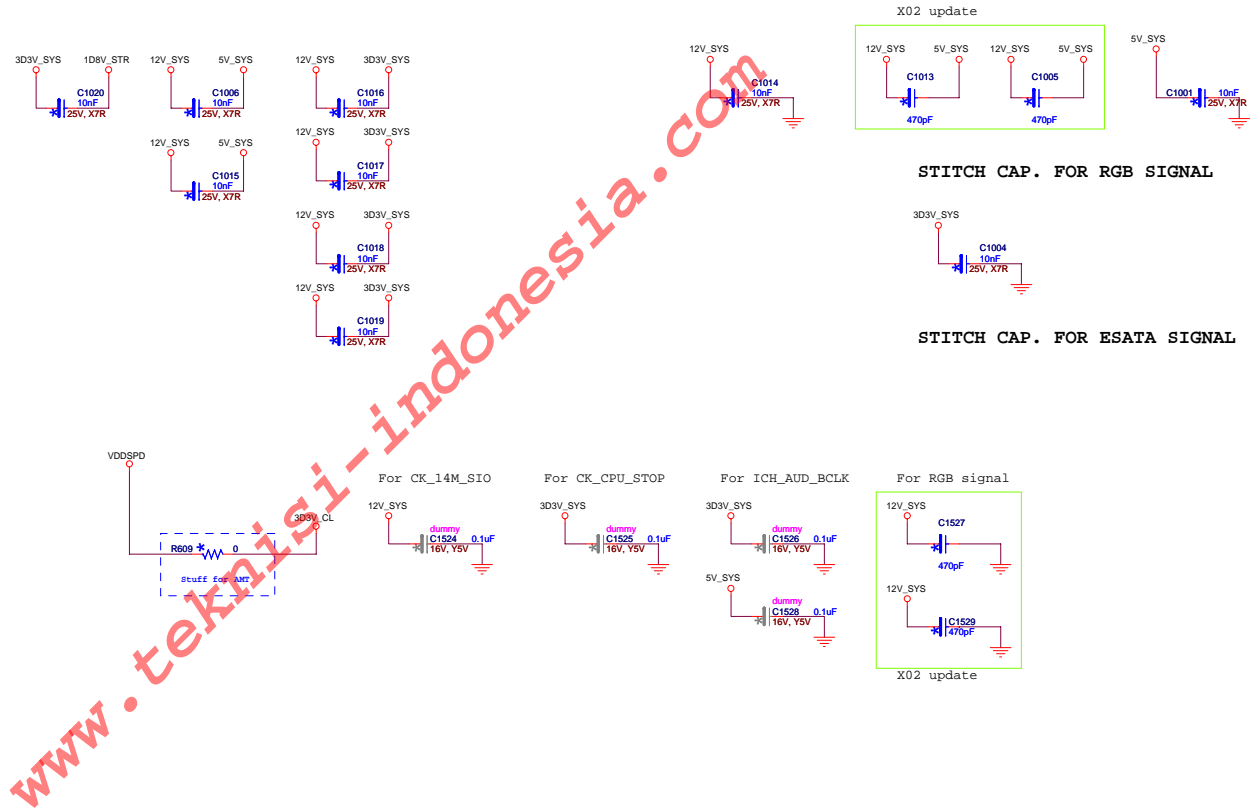


Stuff for AMT

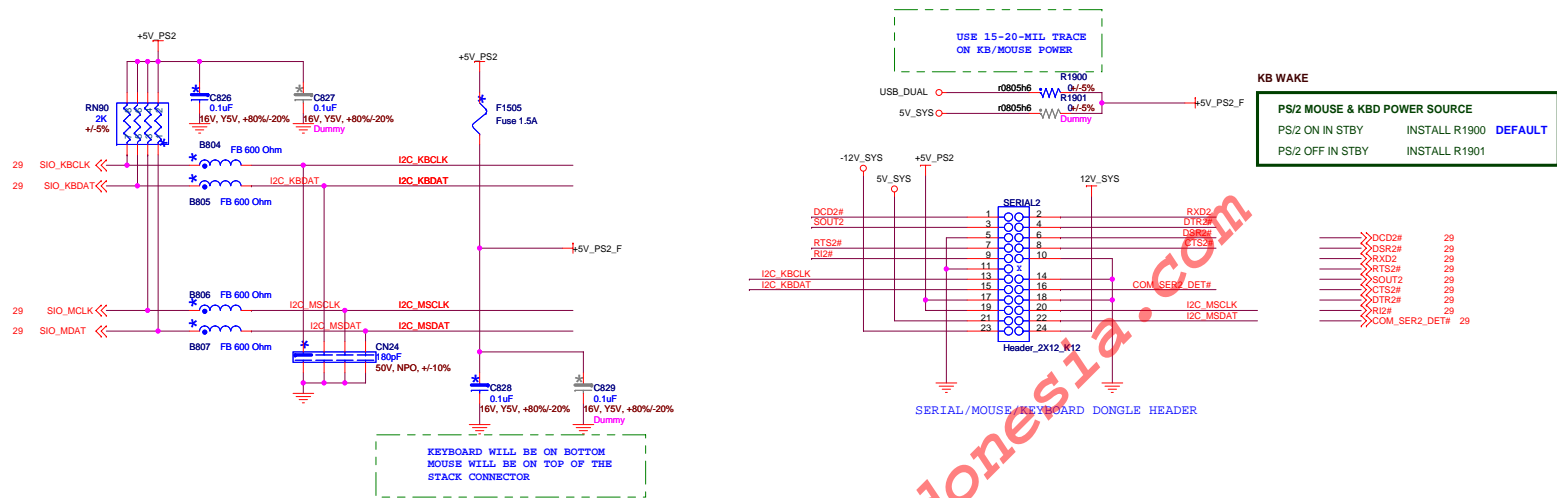


DELL INC.	
Title Reserved-1	
DWG NO GAO	Rev A00
Date Monday, September 01, 2008	Sheet 38 of 45

TP99 ○ TEST1_DUMMY_TOP
TP100 ○ TEST2_DUMMY_TOP
TP101 ○ TEST3_DUMMY_BOT
TP102 ○ TEST4_DUMMY_BOT



KB / MS + COM2 Connector

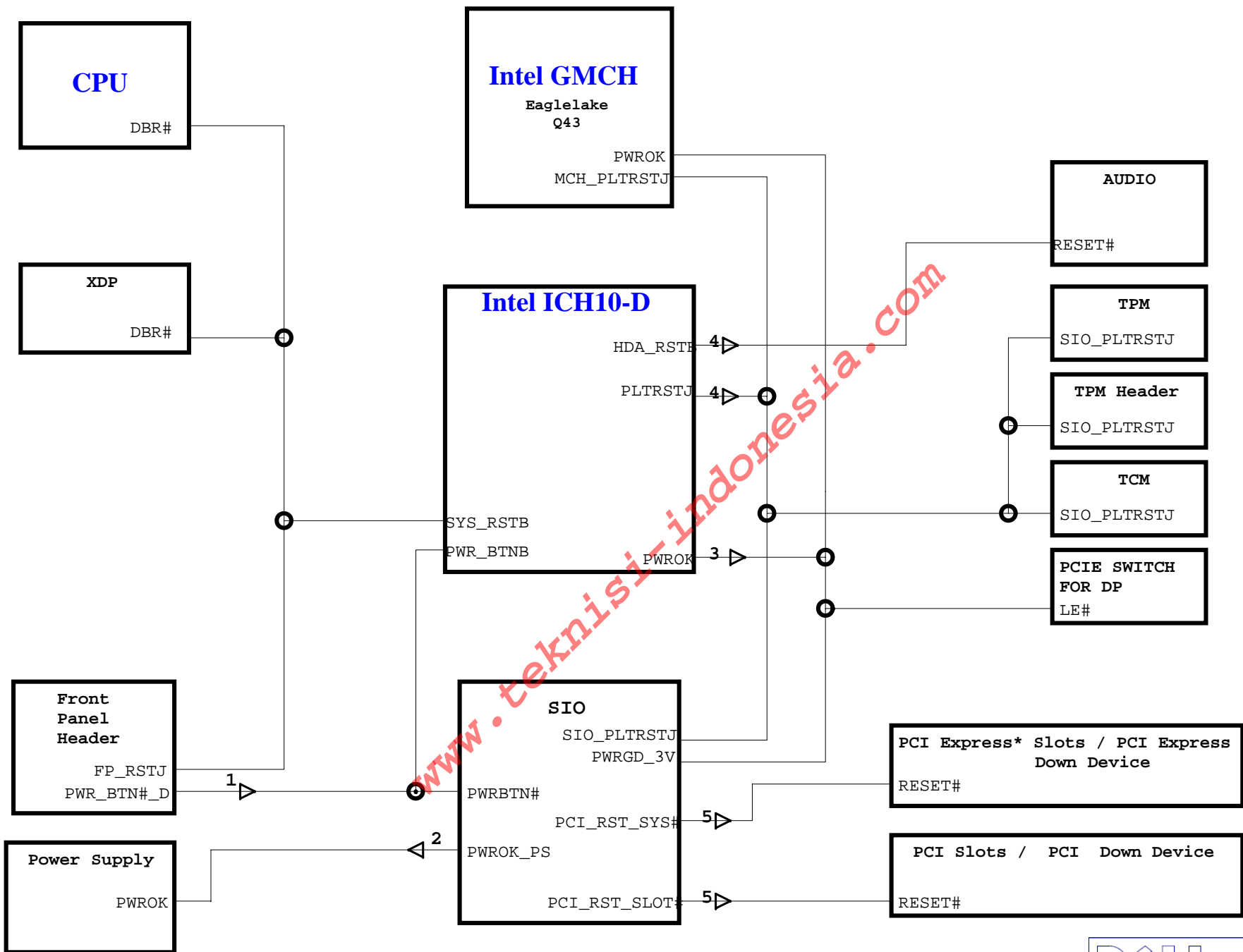


PCI Routing Summary

	PCI0	PCI1				
INTAJ	A	C				
INTBJ	B	D				
INTCJ	C	A				
INTDJ	D	B				
INTEJ						
INTFJ						
INTGJ						
INTHJ						

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 INC.	
Title	
IRQ Map	
DWG NO	Rev
GAO	A00
Date: Monday, September 01, 2008 Sheet 41 of 45	



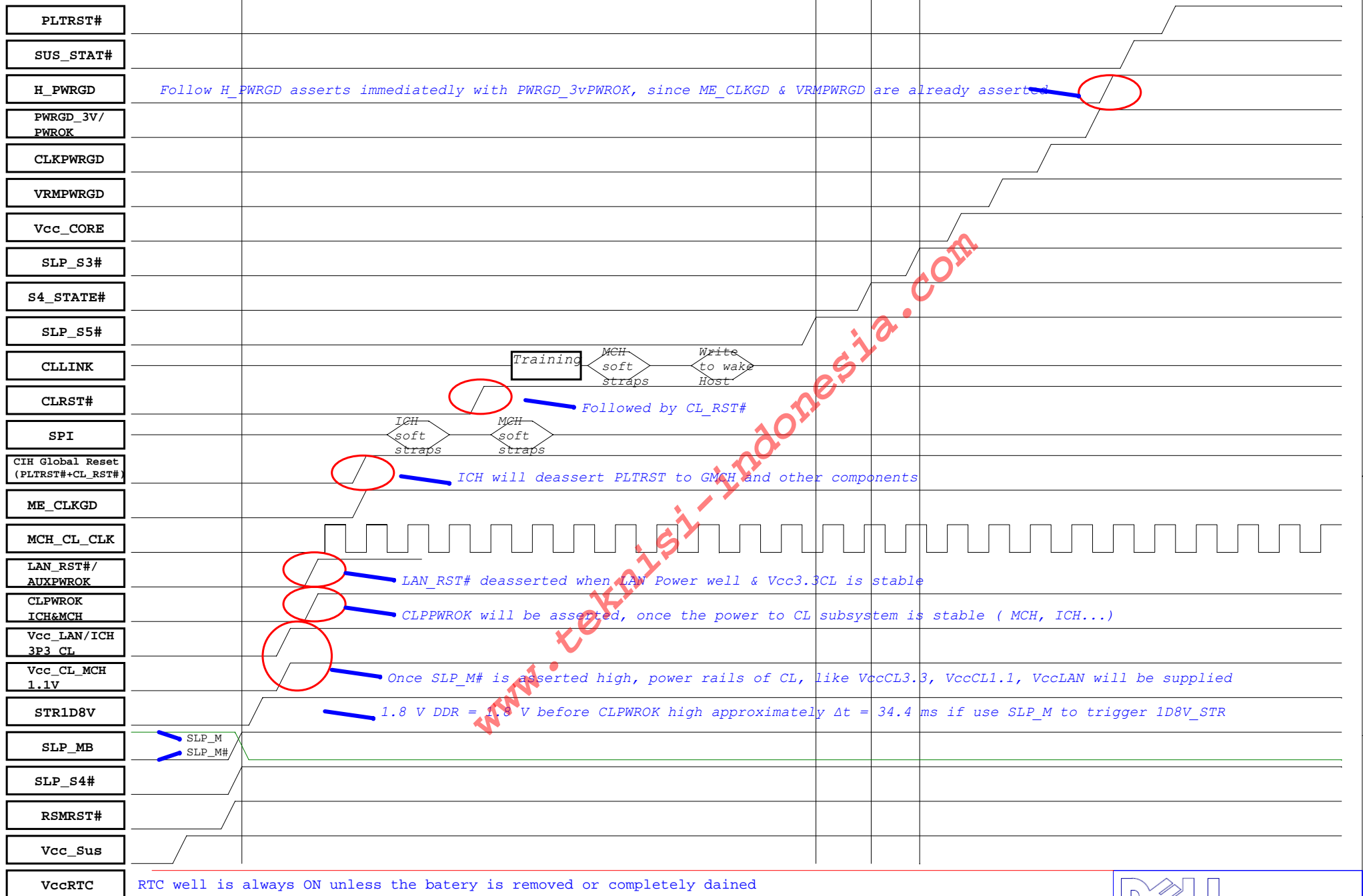
G3/M-OFF

S5/M1

S4/M1

S3/M1

S0/M0



RTC well is always ON unless the battery is removed or completely drained

Title
AMT TIMINGDWG NO
GAORev
A00

Clock Gen IDTCV184 Functional Straps

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	CK_PIN4	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI3/CPGP (PIN5)	CK_PIN5	1	CGP TABLE ENABLED
		0	CGP TABLE DISABLED DEFAULT
PCI4/SRC5_EN (PIN6)	CK_PIN6	1	SRC5
		0	CPU_STOP# and PCI_STOP# DEFAULT
PCI_F5/ITP_EN (PIN7)	CK_PIN7	1	CPU_ITP DEFAULT
		0	SRC8

SIO SMSC5524 Functional Straps

PIN NAME	NET		Strapping description
SPEAKER[DIAG_EN#] /GP8051_45/GPI4 (PIN127)	SPEAKER	1	Diag.En Disable
		0	Diag.En Enable DEFAULT
RTS1#[SYSOPT] /GP8051_58 (PIN101)	RTS1#	1	Sysopt strap 0 X 4E
		0	Sysopt strap 0 X 2E
DTR1#[FLASH_EN] /GP8051_16 (PIN104)	DTR1#	1	Flash Enable
		0	Parallel Enable DEFAULT

Intel ICH10 Functional Straps

PIN NAME	NET		Strapping description
TP3	TP68	1	Danbury Technology Enable Internal Pull-up
		0	XOR Chain Entrance
SPKR	SPKR	1	NoReboot mode Internal Pull-up
		0	Reboot mode
GPIO33 / HDA_DOCK_EN#	MFG_MODE	1	MEEnable DEFAULT
		0	ME disable
SPI_MOSI	ICH_SPI_MOSI	1	MCH TPM Enable
		0	MCH TPM disable DEFAULT

Intel MCH Eaglelake Q43 Functional Straps

PIN NAME	NET		Strapping description
cen	TLS	1	TLS Enable
		0	TLS disable
iTPMb	ITPM_EN	1	iTPM Enable
		0	iTPM disable
DDPC_CTRLDATA	DDPC_CTRLDATA	1	SELECT Display Port
		0	SELECT PCIEX16
DDPC_CTRLCLK	DDPC_CTRLCLK	1	SELECT Display Port
		0	SELECT PCIEX16

Chassis	SKU	TPM	TCM	R543	TPM SKU ID					Board ID		
					SKU3	SKU2	SKU1	SKU0	Pop option	REV1	REV0	Pop option
Smith	1	V	X	Stuffed	0	0	0	0	Stuff R2577, R2582, R2013, R2335	0	0	stuff R2001, R2334
Smith	2	X	X	Stuffed	0	0	1	0	Stuff R2313, R2577, R2013, R2335	0	0	stuff R2001, R2334
Smith	3	X	V	Stuffed	0	0	0	1	Stuff R2576, R2582, R2013, R2335	1	1	stuff R2324, R3334
Neo	4	V	X	Stuffed	0	0	0	0	Stuff R2577, R2582, R2013, R2335	0	0	stuff R2001, R2334
Neo	5	X	X	Stuffed	0	0	1	0	Stuff R2313, R2577, R2013, R2335	0	0	stuff R2001, R2334
Neo	6	X	V	Stuffed	0	0	0	1	Stuff R2576, R2582, R2013, R2335	1	1	stuff R2324, R3334
Cypher	7	V	X	Stuffed	0	0	0	0	Stuff R2577, R2582, R2013, R2335	0	0	stuff R2001, R2334
Cypher	8	X	X	Stuffed	0	0	1	0	Stuff R2313, R2577, R2013, R2335	0	0	stuff R2001, R2334
Cypher	9	X	V	Stuffed	0	0	0	1	Stuff R2576, R2582, R2013, R2335	1	1	stuff R2324, R3334

Chassis	Chassis ID			
	ID2	ID1	ID0	Pop option
Smith	0	1	0	Stuff R2346, R418, R2349
Smith	0	1	0	Stuff R2346, R418, R2349
Smith	0	1	0	Stuff R2346, R418, R2349
Neo	0	0	1	Stuff R396, R2347, R2349
Neo	0	0	1	Stuff R396, R2347, R2349
Neo	0	0	1	Stuff R396, R2347, R2349
Cypher	0	0	0	Stuff R2346,R2347, R2349
Cypher	0	0	0	Stuff R2346,R2347, R2349
Cypher	0	0	0	Stuff R2346,R2347, R2349



X00	<p>1703/19/08*Connect net CK_P8_100M_P_16PORT_A, CK_P8_100M_R_16PORT_B to U1.33,U1.32</p> <p>Connect net CK_P8_100M_P_1PORT_1_P, CK_P8_100M_R_1PORT_1_P to U1.17,U1.18*Deep PCIx16 clk to SRMCI, and PCIx1 clk to SRMCI, because clk from SILEDO does not support GEM if connection on SRMCI</p> <p>23003/19/08*Change R653 to 0 ohms and Q101 to 2M7002*Fixolve DP issue</p> <p>13003/19/08*dummy R673 solve PCIx16 Detection Issue</p> <p>42003/19/08*Change C97, C98 to R268, R269*Change audio capacitor from MLC2 to KCM2 to solve audio quality issue</p> <p>5203/19/08*dummy R410, R421, C145, C156, U10, R414, R416</p> <p>Add Pull from 3DV_VDD to 3DV_VDD to design 0 Ohm and R2117 for Coat down purpose</p> <p>6303/19/08*Remove R307, add R134, R135, R137, R1750*design serial resistor and common choke on USB</p> <p>7603/19/08*Remove R239, add R384, R378, R392, R394</p> <p>Remove R840, add R442, R429, R424, R398</p> <p>Remove R811, add R41, R138, R176, R169*Co-design serial resistor and common choke on USB</p> <p>8203/19/08*Remove R381, add R581,R577, R585, R5870*design serial resistor and common choke on USB</p> <p>9403/19/08*Change SATA1L data signals to net SATA_R0ST, SATA_R0PS, SATA_T0ST, SATA_T0PS*Change SATA data signal from SATA74 to SATA5</p> <p>10203/19/08*Change PCIx1 data signals to net R01_R02, R01_P2, R00_R02, R00_P2*Change PC1x1 signal from port1 to port2</p> <p>11303/19/08*Remove P0R02 and related circuit Remove micro power connect on Smith circuit</p> <p>12203/19/08*Add TP111 on Q101.4*Remove micro power connect on Smith circuit</p> <p>13203/19/08*Delete R1314 and Add C141 diode between R101 pin P0CT_R0CM and ICH10(GP0)SRMC vender feedback* add diode to protect reverse signal from SIO to ICH10</p> <p>14203/19/08*Stop net GP_VGA_CML_H0T3 connection from pin R11 to pin R40*Follow Fleming VMA detection Pin connection</p> <p>15203/19/08*connect U15.15 to 3DV_VB and dummy C143, U8, R195, R194*dummy U8 and connect U15 pin 15 to 1.35k for coat down issue* DC-TO-DC request</p> <p>16203/19/08*dummy Q101, R439, R441, R440, stuff #1920SRMC vender feedback connect P0CT_READY to CPU_L2 and MCH_P42</p> <p>17203/19/08*Change R555, stuff R649 and connect R649 to 3DV_VB instead*Follow Intel latest signing update</p> <p>18203/19/08*Stop QP1024 and QP1026 of ICH10 to fix AMT issue*fix AMT issue</p> <p>19203/19/08*Change R57 and R53 to 10k, stuff R47 and R48*Follow Dell SR Scan request</p> <p>20403/19/08*Change GP1, GP6, GP7 to net TPM_SR03, TPM_SR02, TPM_SR01</p> <p>Add dummy resistors R2213 R207 R1311</p> <p>Add R2582, R2213, R2335*to meet TPM 5 SRU request</p> <p>21203/19/08*Remove R617, R618, R619, R620, R621, R622, R623, R624, C576, C577, C578, C579*Dell Jealy: Please help remove dummy resistors (R617-624) and caps (C576-579) which reserved on LAN MDI circuit from schematic and board file. It seems we don't need it anymore. Also please make sure no changes to MDI signal trace layout when delete these resist.</p> <p>22403/19/08*Delete history at the end of sheet*Foxconn confirmed to add on history data on Q128</p> <p>23103/19/08*Create pop table for reference*Foxconn confirmed to add on pop option on Q128</p> <p>24203/19/08*Add page no on block diagram*Foxconn confirmed to add on page number on Q128</p> <p>25203/19/08*Wrong Q128PF table*Foxconn modified on Q120</p> <p>26203/19/08*Add a series 2 ohm to the GP1_P0CTV_DET signal so this signal can be disconnected as we plan to use the floppy drive detection in the SIO. R2276 should be on the floppy connector side of this series</p> <p>resistor Foxconn modified by adding on R147 on Q120</p> <p>27203/19/08*Add D000 Led on 128P*Foxconn confirmed to add pull down</p> <p>resistor R1277 dummy resistor on Q120, Pull-up voltage will be confirmed on Q128</p> <p>28103/19/08*Add D000 Led on 128P*Foxconn modified on Q120</p> <p>29203/19/08*U15. pin4 need RC connect to 5V_VDD, pin15 need bulk cap, need further discuss with DC/DC*Foxconn DC-DC confirms to connect U15.pin4 to 5V_SVS not 5V_DUAL, due to DC-DC concerned.</p> <p>30203/19/08*U15 has already had bulk cap, need DC/DC Foxconn modify by adding C843, C489 on Q120</p> <p>310203/19/08*Add defense design as attached on USB_dial*Foxconn modified by adding on R347 on Q120 R591 and Q47 on Q120</p> <p>32203/19/08*Should not pin 24 of P01 Port connect to GND</p> <p>33203/19/08*Implement L0CTW of SIO as SRMC recommended. And make measurement to confirm no side effect.</p> <p>3330204/18*Change H0R solution for LAN connector to Add L02 circuit on Page 36*</p>
X01	<p>1. Fix R167 Add in and U1u on Server_A and Server_B to fix power noise issue.*1. Add C413 1uF 0603 and C504 0.1uF 0402 Capacitors</p> <p>2. Add C502 1uF 0603 and C505 0.1uF 0402 Capacitors</p> <p>2. P23 Change Q24 from 3904 to 2n7002*Foxconn internal transistor check correction</p> <p>3. P14 Dummy C74 Remove unused capacitor</p> <p>4. P14 L26 Change parts to 0.18 uH (same as Fleming) Change inductor to fix memory clock jitter fail issue</p> <p>5. P30 Add three more stitching capacitors C1028, C1026, C1027on Display Port Data signal, one capacitor for two signals----- Feedback by Dell Sean</p> <p>6 P07/P34 *Redesign TPM/TCM circuit as Dell reference circuit</p> <p>1. Remove R1155, R135, R137, R396, R331, R218, R403</p> <p>2. Change C57 from 0.1uF to 10uF</p> <p>3. Add C84, C86, C506, R400, R277, R443, R444, R212, R224, R226</p> <p>4. Add net CK_14M_210M, CK_14M_10CM and R1008, R1009, R1006, R1005, R1010, R1011, R1007, C506, C507, C508 and Net CK_14M_TPM</p> <p>5. Change R4, and R14 from 33 ohms to 10 ohms Q402 resistor</p> <p>6. Remove C21 and C27</p> <p>7. Add three capacitors, C513, C514, C515 for 3DV_VYS near TPM package.*1. Modify TPM/TCM circuit to meet Dell requirement.</p> <p>2. For TPM 14M clock signal option</p> <p>3. Adjust damping resistor for additional shared signal to TPM</p> <p>7. P07 *1. Add dummy pull up resistor 10K R535 for net CK_P0CT_STOP_R</p> <p>2. Add dummy pull up resistor 10K R606 for net CK_CPU_STOP_R*Change refer to Intel C5X05 PCI_STOP# and CPU_STOP# Termination Rev.1.1</p> <p>8 P27/P36 *1. Change 3DV_VCL decoupling capacitors C129,C142 and C412 from 0.1uF to 120pF</p> <p>2. Change VCT decoupling capacitor C417 from 4.7uF to 1uF</p> <p>3. Change LAN_10BV decoupling capacitors C425,C426 and C427 from 0.1u to 120pF</p> <p>4. Add decoupling capacitor C501 120pF on LAN_10BV</p> <p>5. Add decoupling capacitor C1021 10uF on LAN_R0ST Parallel with R616) *RBD improvement</p> <p>9. P22/P30 *Redesign Display port related circuit reference Fleming 0518 schematic</p> <p>1. Change R674 to 0 ohms and Q66 to 2N7002 to increase net DP_P13_IRV voltage level.</p> <p>2. Add stitch capacitors C1021, C1021, C1024, C1036, C1027</p> <p>3. Reserve decoupling capacitors C516 0.1 uF, C499 10uF for DP connector.</p> <p>4. Reserve decoupling capacitor C1002 1uF for net DP_P13*To fix motherboard Display priority function issue</p> <p>10. P23/P24 *SRU GP10 change</p> <p>- TPM_SR03 change to GP1_SR02 to GP10 27</p> <p>- TPM_SR03 to GP1_SR03 to GP10 72</p> <p>- TPM</p> <p>- GP4 to MC_P10SR02A_CML_H0T3 pull high R1013 10k ohms to 3DV_VYS</p> <p>- GP4 to MC_P10SR02A_CML_H0T3 pull high R1012 10k ohms to 3DV_VYS</p> <p>- Remove R2013, and R2335, TP200*Change GP10 pins same as Fleming</p> <p>11. P23 Add R1014, reserve R1015, Q111 connect R1014 to net SLP_M_GATE and Q111.R444 circuit to solve ME (LAN_PWR0K) power sequence issue</p> <p>12. P25 Remove circuit: C143, U8, R195, R194*Remove unused LDO circuit for 5V_UB to 3DV_VB</p> <p>13. P36 Remove D20, R596 and R600*Remove D20, R596 and R600 and modify U3522 pin1 and 1 input circuit more clearly-----feedback by Dell Jealy</p> <p>14. P27*Remove TP52 TP53 TP55 TP56 TP57</p> <p>Add R1015, R1016, R1020 51 ohm resistors pull up to 3DV_VCL and R1017 R1018, R1019 51 ohm resistors (dummy R1019) pull down to GND *</p> <p>RBD solution: P27 Pull down J7CM, J7D0, J7B0T (for option) with 51 ohm resistors. Pull up J7PM, J7D1, J7B0T with 51 ohm resistors. -----feedback by Dell Jealy</p> <p>15. P28 Change R127 from 10 ohms resistor to 100 ohms resistor and C300 from 0.1uF 5V5 Q402 to 1 uF XSR 0603 capacitor. Delete D11 and replace it with Q99 Target to meet V558F_S09 Ramp Rate Requirement on ICH10D-----Suggestion given by Intel T.S.</p> <p>16. P30 Add 1M ohms resistor, R3888 on DP_P0CT1 pin 14*Follow Fleming 0518 schematic Design--- Feedback by Dell Sean</p> <p>17. P1011 and U12 component change 74ACCT100R06</p> <p>18. P30 *1. remove Q101 and Q81, reserve Q1042 instead</p> <p>2.remove U1514 and change related circuit to Q90, Q91, Q92, Q93, Q94, Q95, Q96, Q99*</p> <p>19. P14 remove R42, reserve R598</p> <p>20. change 14.318 circuit design with 15 ohms damping resistors. one to three (SIO ICH TPM)</p>
A00	<p>1. P20 Change R197 from 4.7 to 8.2K Follow Fleming design</p> <p>2. P23 1. Change R152 from 237 Ohm to 150 Ohm 2. Add R264, R401 and C559, R2018, Q112 and Q113 (NCL_N0L to control LAN_PWR0K timing) Follow Fleming design</p> <p>3. P24 1. CL. Dummy R3334. 2. Change board rev ID. Follow Fleming design</p> <p>4. P24 Update SRU table Follow Fleming design</p> <p>5. P27 Dummy C1021 Fix IEEE BEB issue</p> <p>6. P30 Change R674 from 8.2K to 0 Ohm It's risky to turn Q66 on as R674 is 8.2K.</p> <p>7. P34 Fix LDC bus design error on X01 Fix LDC bus design error on X01</p> <p>8. P14 Remove P099 on R334 Follow Dell's request.</p> <p>9. P38 Change C51 2N7002 to 2N3904 Fix ME sequence issue</p> <p>10. P39 VGA stitching capacitors: 1. Add C1527 and C1529 470pF 2. Change C1013 and C1005 from 10uF to 470pF Fix VMA DMI 192MHz Issue</p> <p>11. P20,P26,P27 Change C129, C142 and C412 from 120pF to 0.1uF Follow Jealy's request.</p> <p>12. P27 Change LAN_10BV decoupling caps C425, C426 and C427 from 120pF to 0.1uF Follow Jealy's request.</p> <p>13. P36 Change VCT decoupling caps C417 from 1uF to 4.7uF Fix LDC bus Follow Jealy's request.</p> <p>14. P10 Change C32 to R195 1.5K ohm and dummy R107.</p> <p>15. P8 Change R586 from 1K to 200 Ohm and C191 from 22n to 4.7nF.</p> <p>16. Remove P092 option.</p> <p>1. P27 stuff R555 LAN_READABLE connect to ICH Follow Fleming design</p> <p>2. P29 *SIO signal S07T2 and D7524 pull up resistor value increase from 30K to 88.7K to Reduce PWR_GOOD_3V glitch during AC power ON--R170 ID D718423</p> <p>3. P30 dummy R403 and stuff R415 with Q402 0ohms *GEMH1 SMITH PIN L88 connect to GND Follow Fleming Design *</p> <p>4. P33 change R3840 from 39K to 33K, and R3839 from 39K to 20K 0603 resistors Change FAN_ID_Voltage Divider resistors value to 33K and 20K ohm Follow Fleming Design</p> <p>5. P10 dummy R85 Unstuff Pull up resistor, R85 for net BROCH07T Follow Intel CMB</p> <p>6. P24 dummy C277, C278, C279, C280, SATA2 in Neo and Cypher Dell Required</p> <p>Note.</p> <p>Q1039 in Page29 , SLOTT1 Pin A1 in Page22 , and R1311 in Page24</p> <p>These Circuits will follow Fleming design on version that will change LAYOUT FILE</p>